CHIPS DESIGN CRITICAL REVIEW

Department of Electrical and Systems Engineering

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Top Cell Path:
`/home/home2/team4chips2025/TSMC_180_work/SPECTRUM_ANALYZER/TEAM04_RELEASE`

December 25, 2025

1 Progress

	Sch.	Lay.	PEX
Top Cell	√	√	◯
Serial Input Mem.	√	√	√
Second OpAmp	√	√	√
PLL	√	√	☒
Single to Diff. Conv.	√	√	√
LP Filter	√	√	√
PFD	√	√	√
Mixer	√	√	√
VCO	√	√	√
Divider	√	√	√
Op. Amp.	√	√	√
Diff. to Single	√	√	√

Table 1: √: Finished. ◯: Started but not Finished. ×: Not Started. ☒: Not Possible.

1.1 System Block Diagram

Figure 1: Block Diagram: Signal Path Through the Chip to External ADC

2 Top Cell

2.1 Top Cell Schematics

Figure 2: Top Cell Schematics

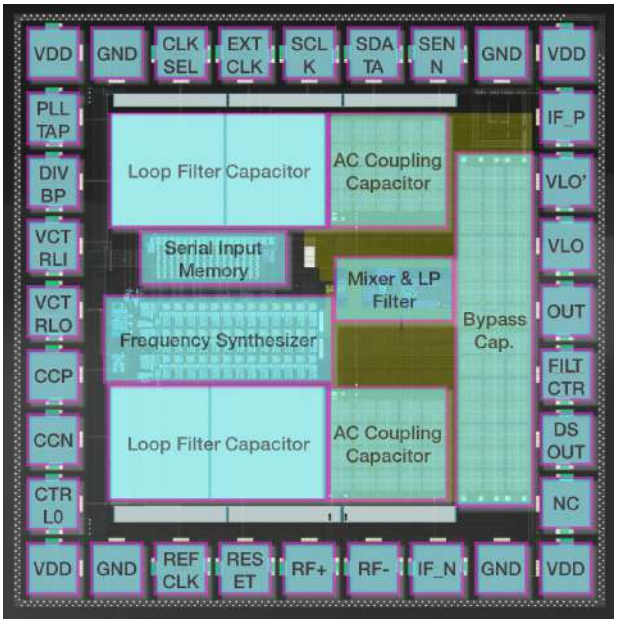

Figure 3: PAD and chip Configuration

2.2 Top Cell Layout

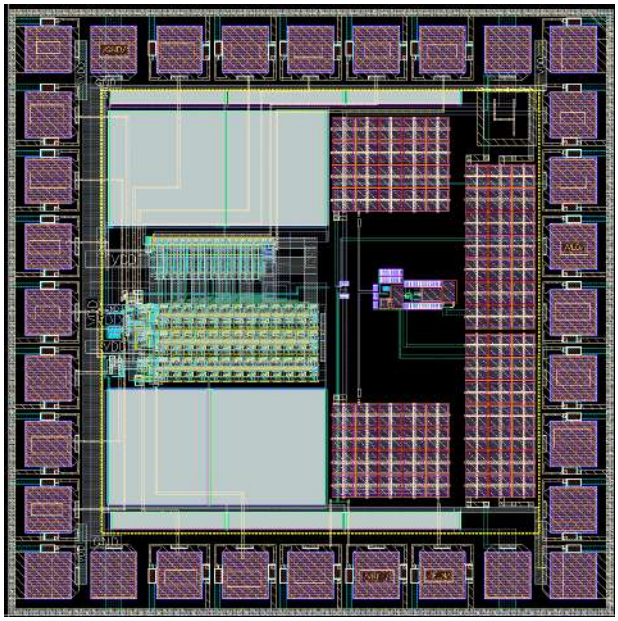

Figure 5: Top Cell Layout

2.3 Top Cell Checks

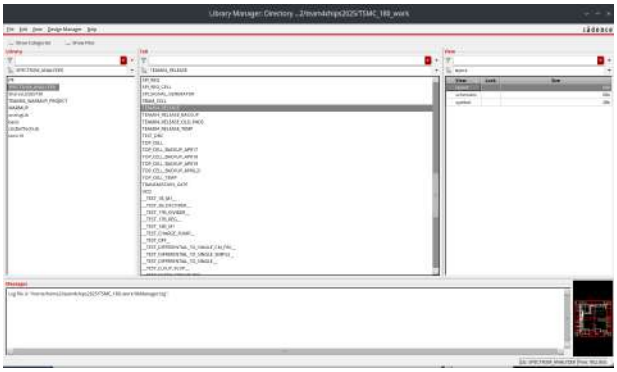

Figure 4: Top Cell File Path

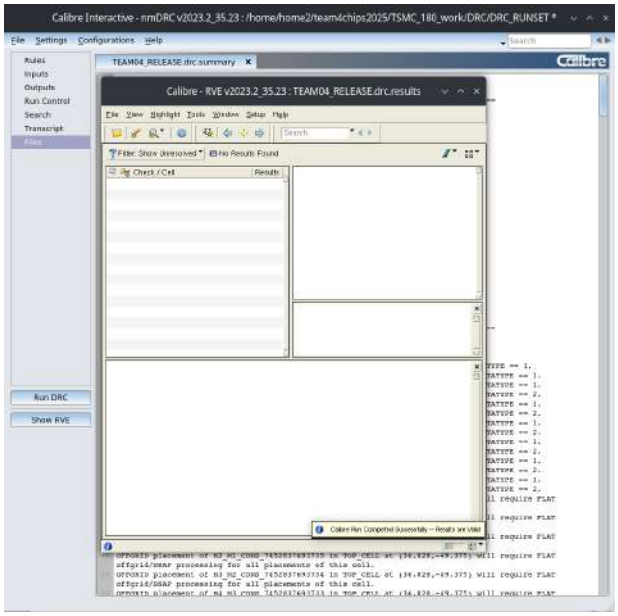

Figure 6: DRC Calibre

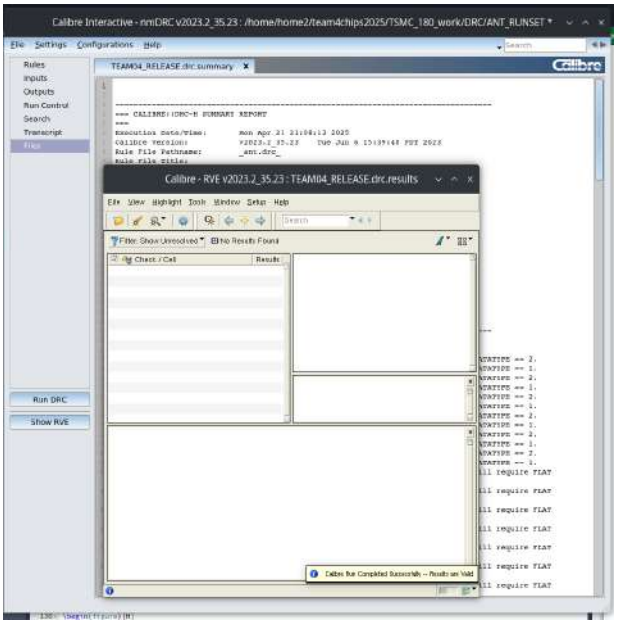

Figure 7: TOP CELL ANT DRC

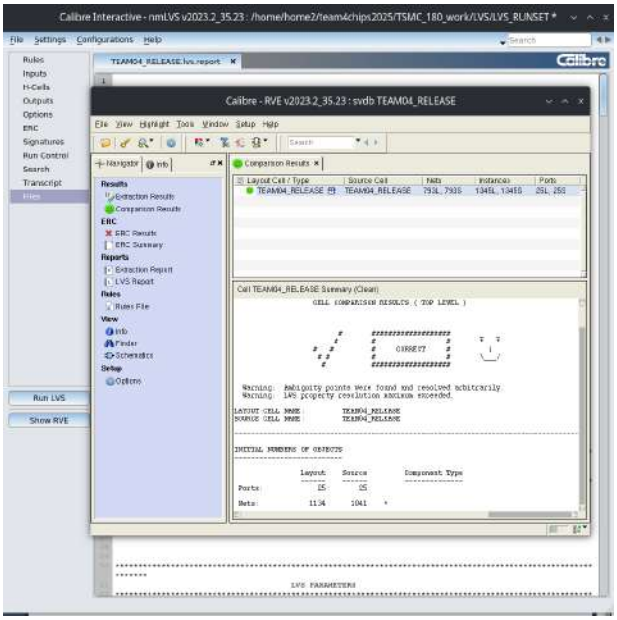

Figure 8: LVS TOP Cell

3 PLL

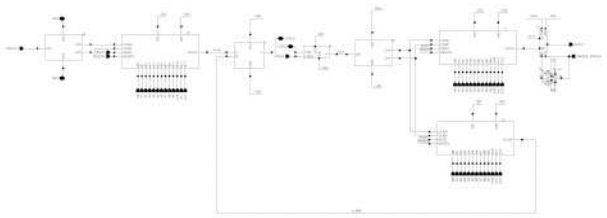

Figure 9: Schematic of the PLL

Figure 10: Layout of the PLL

3.1 Overview

The top cell consists of a circuit made up of NMOS and PMOS transistors. We analyze it below.

4 Serial Input Memory

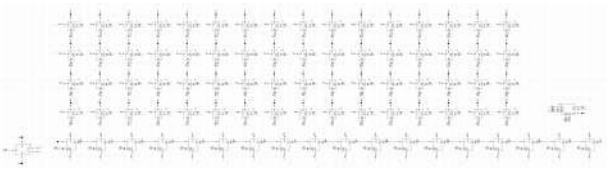

Figure 11: Schematic of the Serial Input Memory

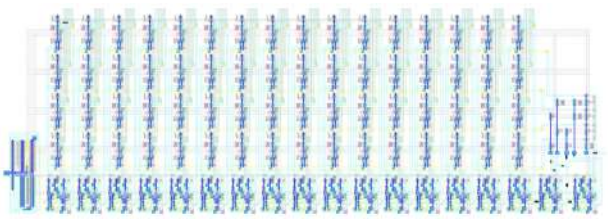

Figure 12: Layout of the Serial Input Memory

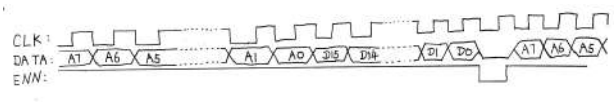

Figure 13: Time Diagram of the Serial Input Memory

Below is a test block to generate the timing for testing serial input memory.

```
module CONFIG_SIGNAL_GENERATOR(inout VDD,
inout GND, output DATA, output CLOCK,
output EN);
parameter real Frequency = 10M;
parameter string A00 = "5A5A";
parameter string A01 = "0A0A";
parameter string A02 = "0505";
parameter string A03 = "1A1A";
parameter real Rise_Time = 1p;
parameter real Fall_Time = 1p;
electrical VDD, GND, DATA, CLOCK, EN;
real vlow = 0;
real vhigh = 1.8;
integer datapin = 0;
integer clkpin = 0;
integer enpin = 1;
integer d = 0;
integer data[0:3];
integer a = 0;
integer datap = 1 << 23;
integer cycleCnt = 0;
integer clkDisable = 0;
analog begin
 V(CLOCK) <+ transition(clkpin ?
(clkDisable ? vlow : vhigh) : vlow, 0,
Rise_Time, Fall_Time);
 V(DATA) <+ transition(datapin ? vhigh :
vlow, 0, Rise_Time, Fall_Time);
 V(EN) <+ transition(enpin ? vhigh : vlow,
0, Rise_Time, Fall_Time);
 $bound_step(0.1/Frequency);
 @ (initial_step) begin
  vhigh = V(VDD);
  vlow = V(GND);
  $sscanf(A00, "%X", data[0]);
  $sscanf(A01, "%X", data[1]);
  $sscanf(A02, "%X", data[2]);
  $sscanf(A03, "%X", data[3]);
  d =  (a << 16) | data[a];
  datapin = ((d & datap) == 0) ? 0 : 1;
 endused
 @ (timer(0.5/Frequency, 0.5/Frequency, ,
(a=!4))) begin
  clkpin = ~clkpin;
 if (clkpin == 0) begin
  cycleCnt = cycleCnt + 1;
  datap = datap >> 1;
  datapin = ((d & datap) == 0) ? 0 : 1;
  if (datap == 0) begin
   if (enpin == 1) begin
    enpin = 0;
    clkDisable = 1;
   end else begin
    a = a + 1;
    enpin = 1;
    clkDisable = 0;
    datap = 1 << 23;
    d = (a << 16) | data[a];
   end
  end
 end
end
endmodule
```

5 Single to Differential Digital

This block converts a single-ended digital signal into a differential digital pair. We are routing the LO signal from the PLL to this block to make it differential as the LO signal is square wave. This is block give us the expected signal.

For LO we have transmission gate connected with inverter and for LO' we are passing the signal through 2 inverter in series (a Buffer)

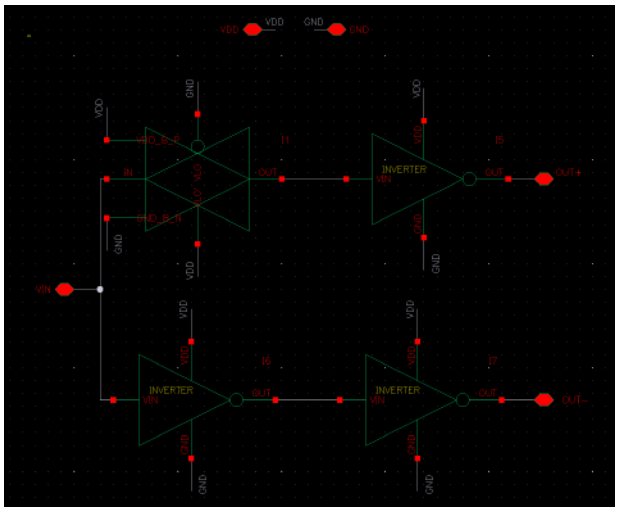

Figure 14: Single to Differential Digital Schematic

5.1 Layout

The physical layout was implemented to ensure symmetrical routing for both differential outputs, maintaining signal integrity. we have used the metal mesh as suggested to surround the smaller blocks to reduce the noise interference.

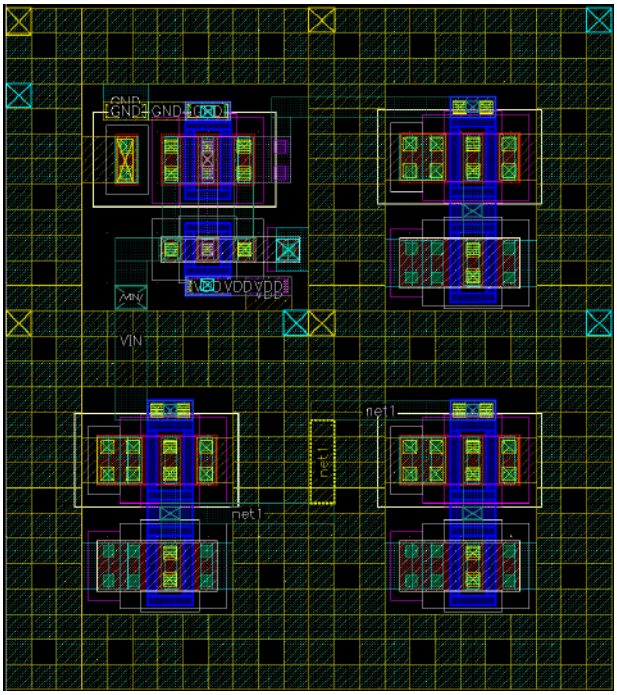

Figure 15: Single to Differential Digital Layout

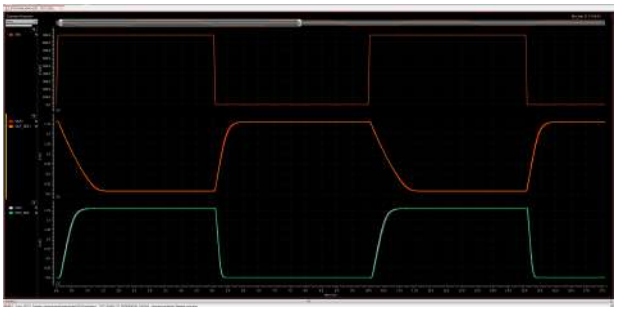

Figure 16: Simulation Results with the PEX Simulation

We can see the PEX results are very close to the simulated result, we tested our single to differential converter with the square wave of amplitude of 1V. And the PEX device can also operate till 100MHz without any issue.

6 Mixer

The mixer is a key component in frequency translation, particularly for down-converting high-frequency RF signals into lower intermediate frequencies (IF) for easier processing.

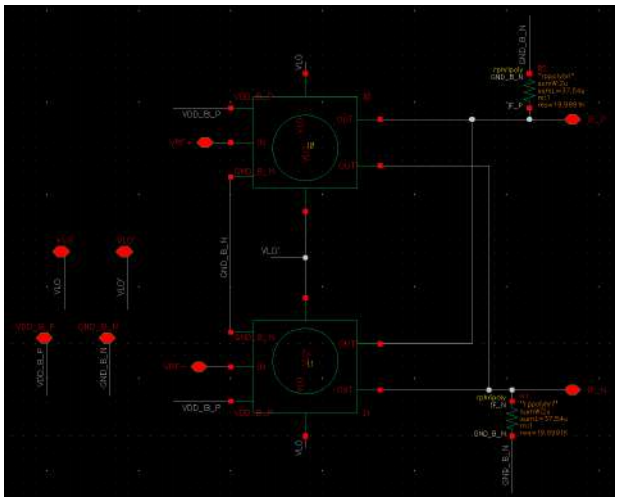

Figure 17: Mixer Schematic

6.1 Layout

A compact layout was designed to minimize parasitic and maintain good matching in the LO and RF paths.

we tested the PEX and simulated results they matched very closely

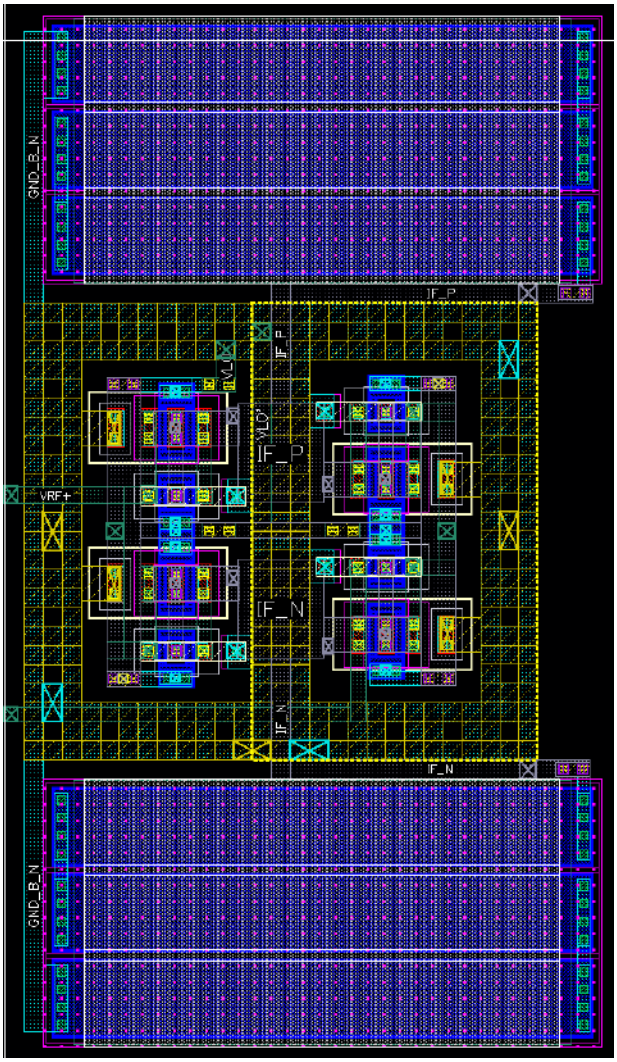

Figure 18: Mixer Layout

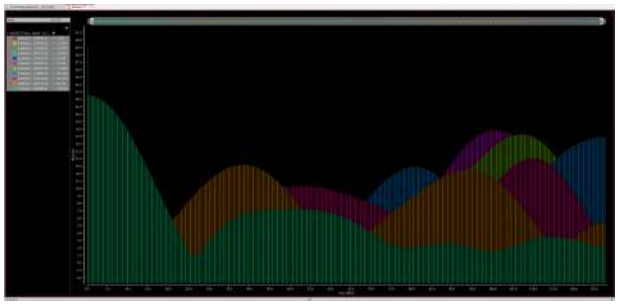

Figure 20: DFT Downconversion

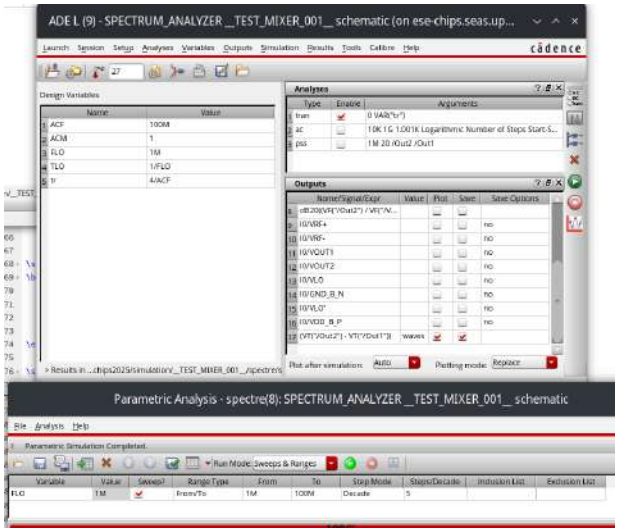

Figure 21: ADL Output

6.2 Testbench & Results

The testbench includes transient, PSS, and frequency-domain simulations to validate the mixing performance, LO leakage, and downconversion effectiveness.

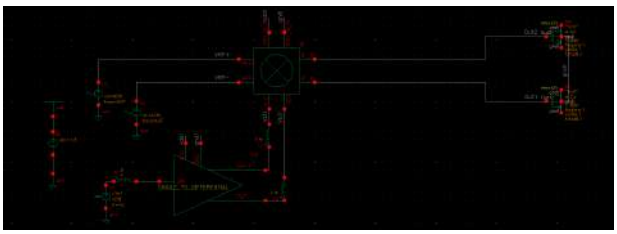

Figure 19: Mixer Testbench – Transient Analysis

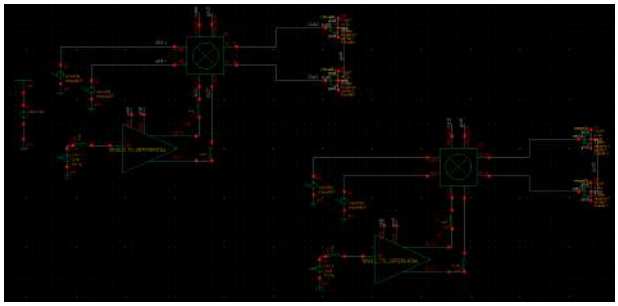

Figure 22: PEX Test on Mixer

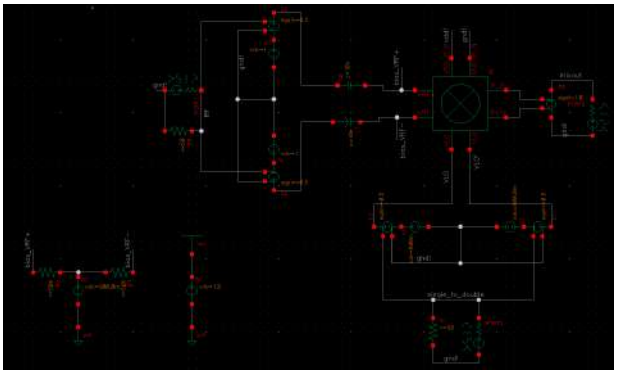

Figure 23: PSS Analysis

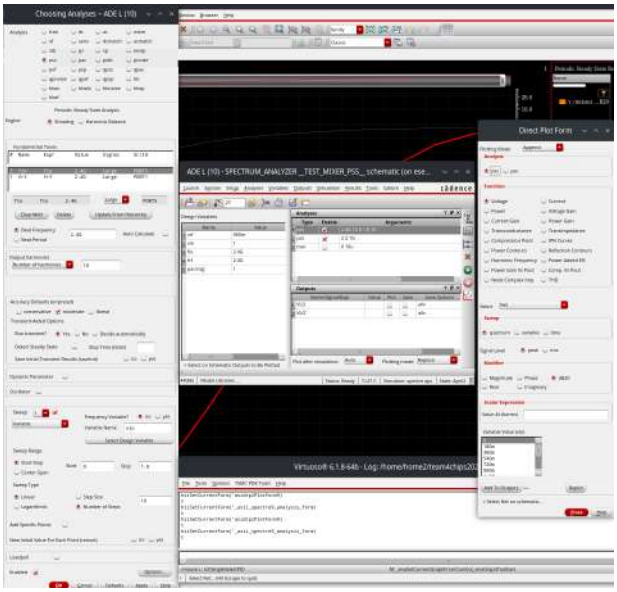

Figure 26: PSS ADL Output

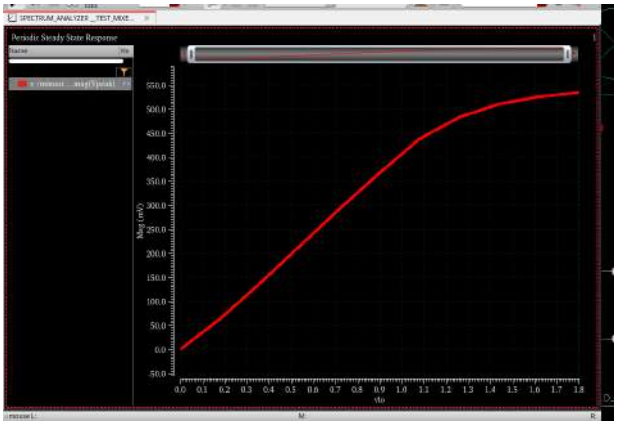

Figure 24: PSS Result

We have test the PEX on the mixer, we want to discuss the PEX results and do an en depth test for this with you to figuer out any possible design issue.

7 Differential to Single Analog

This block converts differential analog signals into single-ended form. It's a critical step for interfacing with single-ended stages, such as ADCs or baseband outputs.

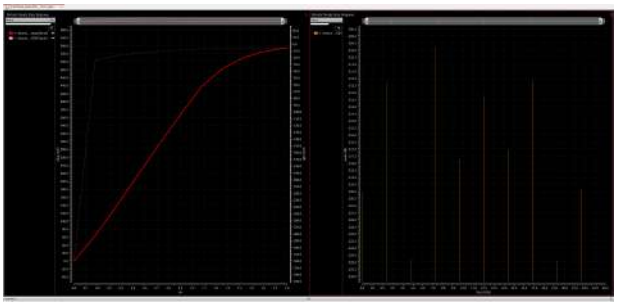

Figure 25: PSS Spectrum

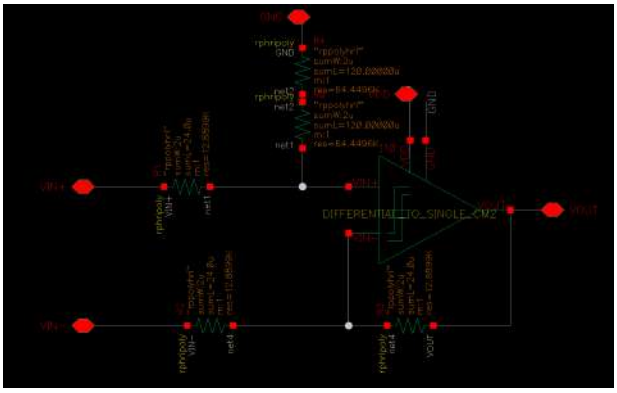

Figure 27: Differential to Single Converter Schematic

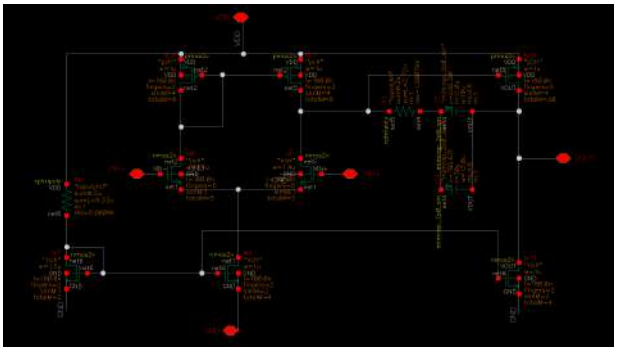

Figure 28: Differential to Single Op-AMP

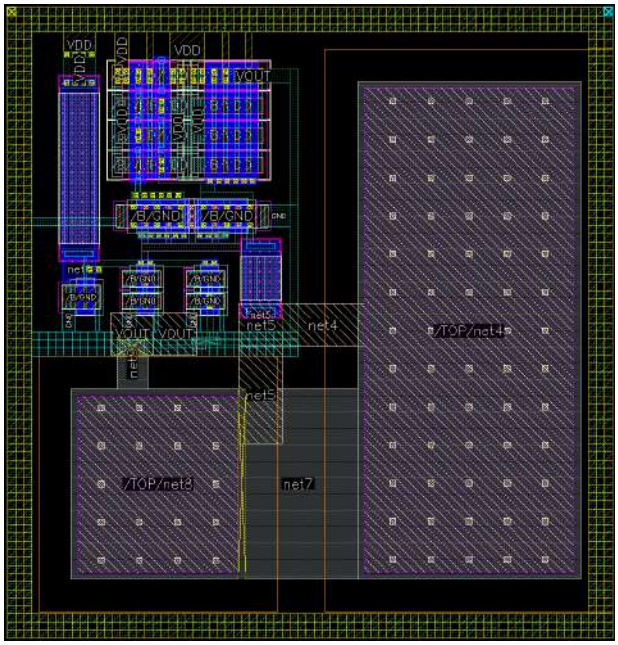

Figure 30: Differential to Single Layout

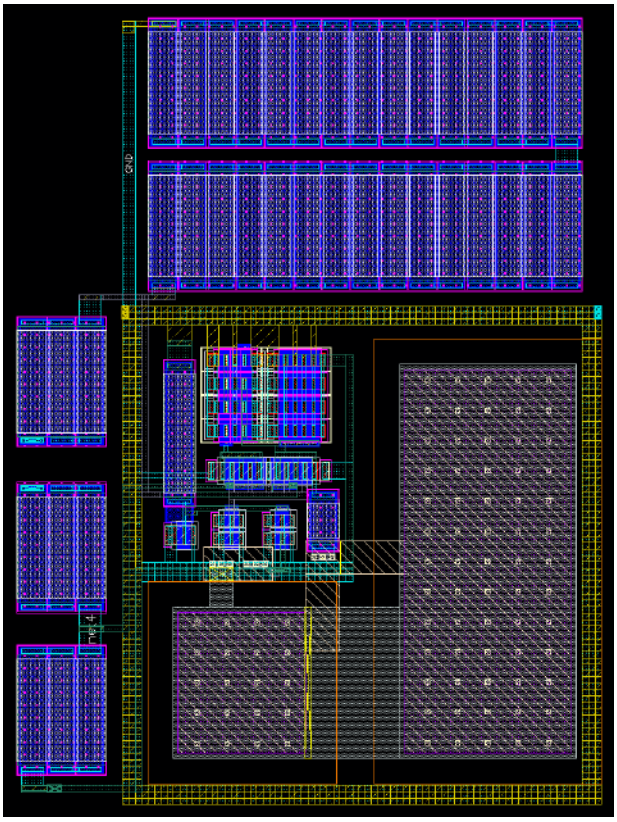

Figure 29: Differential to Single Op-AMP Layout

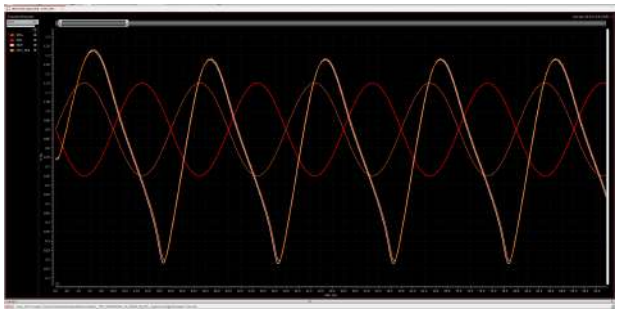

Figure 31: Differential to Single Test Result

We implemented a feedback based differential to single converter, using an high performance opamp. The resistor connected from VIN+ to GND is 128K ohms to keep the voltages up and the remaining 3 resistor are 12K ohms to have sufficient feedback.

8 Filter

The low-pass filter is used to remove high-frequency noise and unwanted mixer products. This filter is based on OP-AMP setup in unity gain configuration

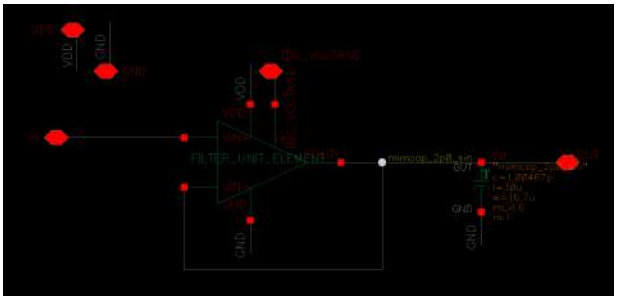

Figure 32: Low-Pass Filter Schematic

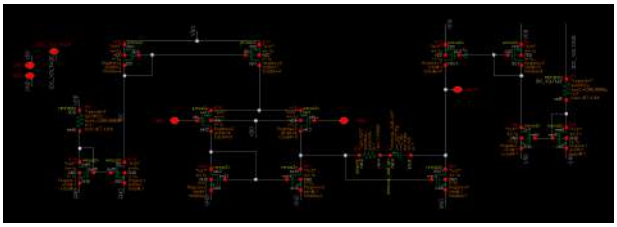

Figure 33: Low-Pass Filter - OPAMP Schematic

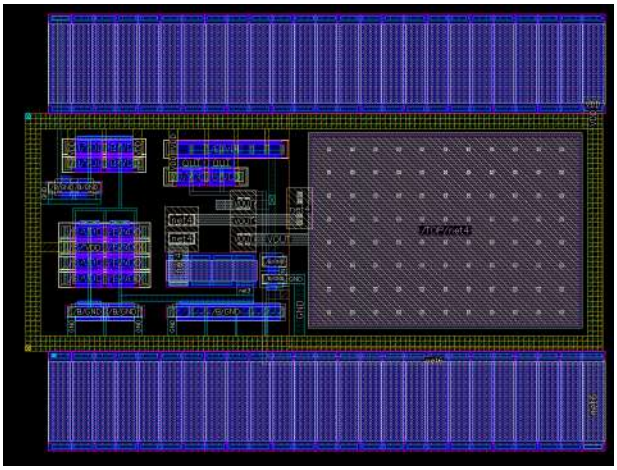

Figure 34: Low-Pass Filter Unit - Layout

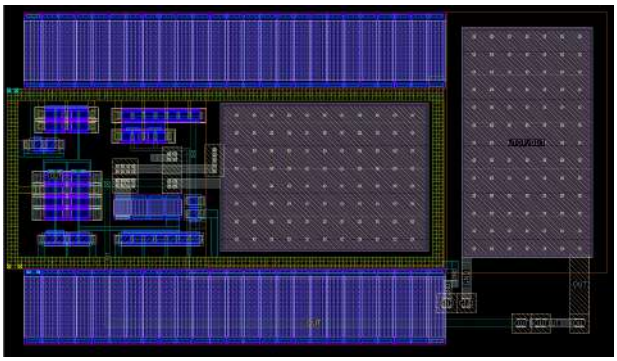

Figure 35: Low-Pass Filter - Layout

8.1 Testbench & Results

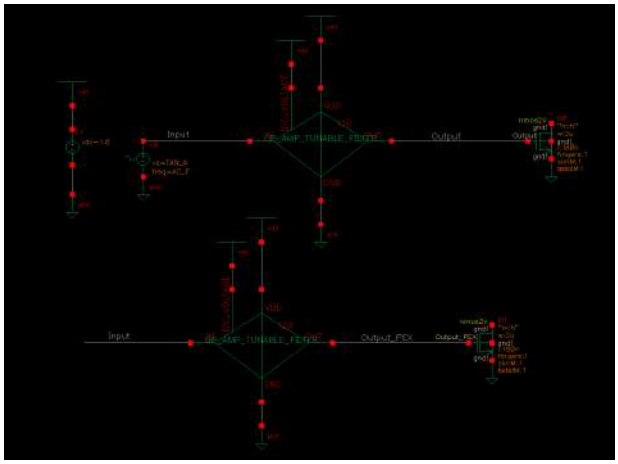

Figure 36: Filter Testbench

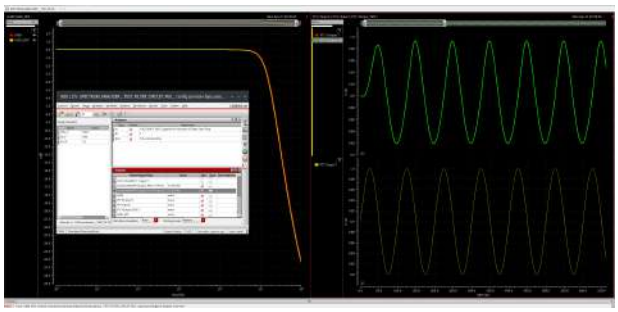

Figure 37: Filter Cutoff Frequency

To make the filter tunable, we plan to vary the IDC current in the second stage. This will allow us to shift the cutoff frequency dynamically depending on the desired signal bandwidth.

9 PEX for Combined Blocks

We did the comparison of the blocks after PEX but weren't able to do the PEX for whole chip because of simulation time and resource constraints.

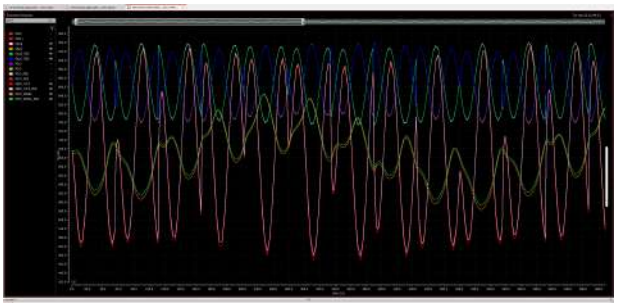

Figure 40: FLO 9MHz and VRF 25Mhz

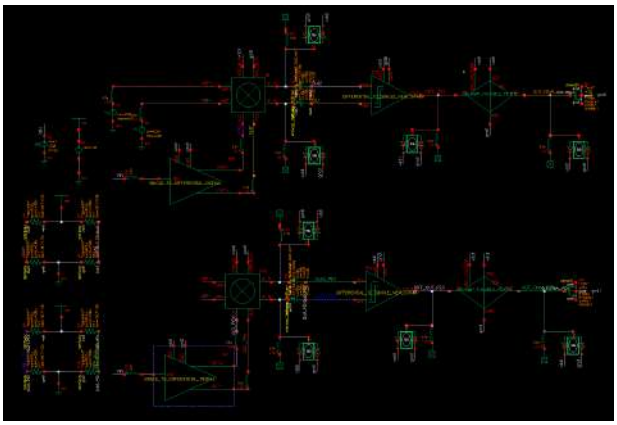

Figure 38: MIXER->Low Pass Filter with PEX

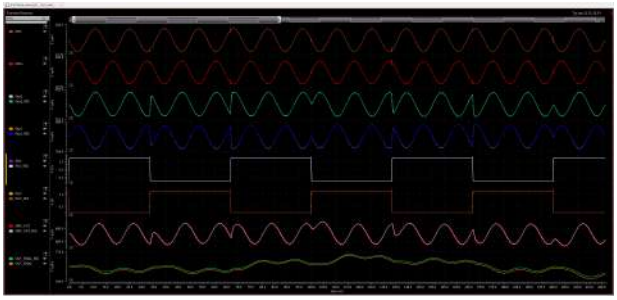

Figure 39: PEX result comparison FLO 15Mhz and VRF 70Mhz

we test with different VRF magnitude and the minimum voltage for the VRF is 100mv if we go below this the output becomes flat.

10 Measurement Plan

For the measurement setup, we plan to generate the input signal using either a **function generator** or

Figure 41: Final Full Simulation

a **microcontroller**, depending on the desired waveform and frequency requirements. This signal will be provided to the input of the chip and then follow the internal signal path as described below:

1. The input signal is first processed by the **PLL**, which generates the necessary LO (local oscillator) signal.
2. The LO signal is then passed through the **Single-to-Differential Converter** to create a differential LO pair suitable for mixing.
3. The differential LO signal and RF input are fed into the **Mixer**, which performs frequency down-conversion.
4. The output of the mixer, which is still in differential form, is sent to the **Differential-to-Single Converter**.
5. The single-ended output from the converter is then filtered using a **Low-Pass Filter (LPF)** to remove unwanted high-frequency components.
6. Finally, the filtered analog signal exits the chip and is passed to an **external ADC** for digitization and further digital processing.

This signal chain allows for full end-to-end evaluation of the chip, from RF input through analog processing to digital conversion.

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Chips Measurement

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Team: 4
TA: Bryce Yu

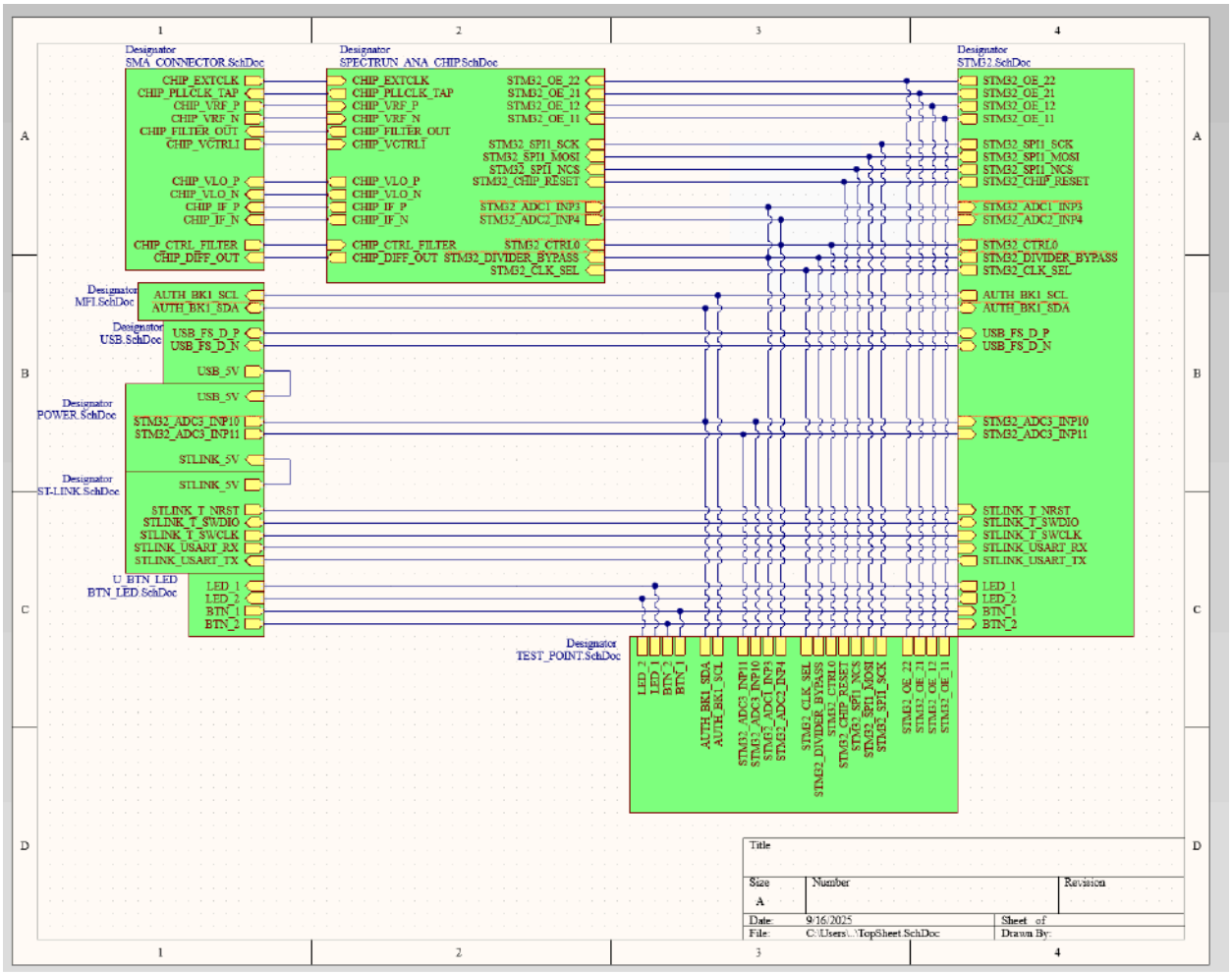


Figure 1: Overview of Schematic

- Spectrum analyzer IC (U4) is the main RF front-end, connected to SMA ports for clock, IF, LO, and test signals.
- STM32 MCU handles SPI control, ADC data, USB, ST-LINK debug, buttons, and LEDs.
- SPI lines (SCK, MOSI, NCS) link STM32 to the analyzer chip.
- ADC inputs capture analog measurements from RF paths.
- USB FS interface provides PC communication; ST-LINK gives programming/debug access.
- Separate power rails: USB_5V, STLINK_5V, regulated supplies for RF and digital.

- SMA connectors require controlled 50Ω traces, short and direct to RF chip.
- RF ground plane must be continuous; use via stitching around SMA and RF chip.
- Decoupling capacitors should be placed close to VDD pins of RF IC and MCU.
- Keep digital and RF sections isolated; route USB differential pairs with matched length.
- Test points added for SPI, reset, LEDs, and buttons for debugging.
- Layout groups: RF front-end on left/top, digital control bottom/right, power regulation top/mid.

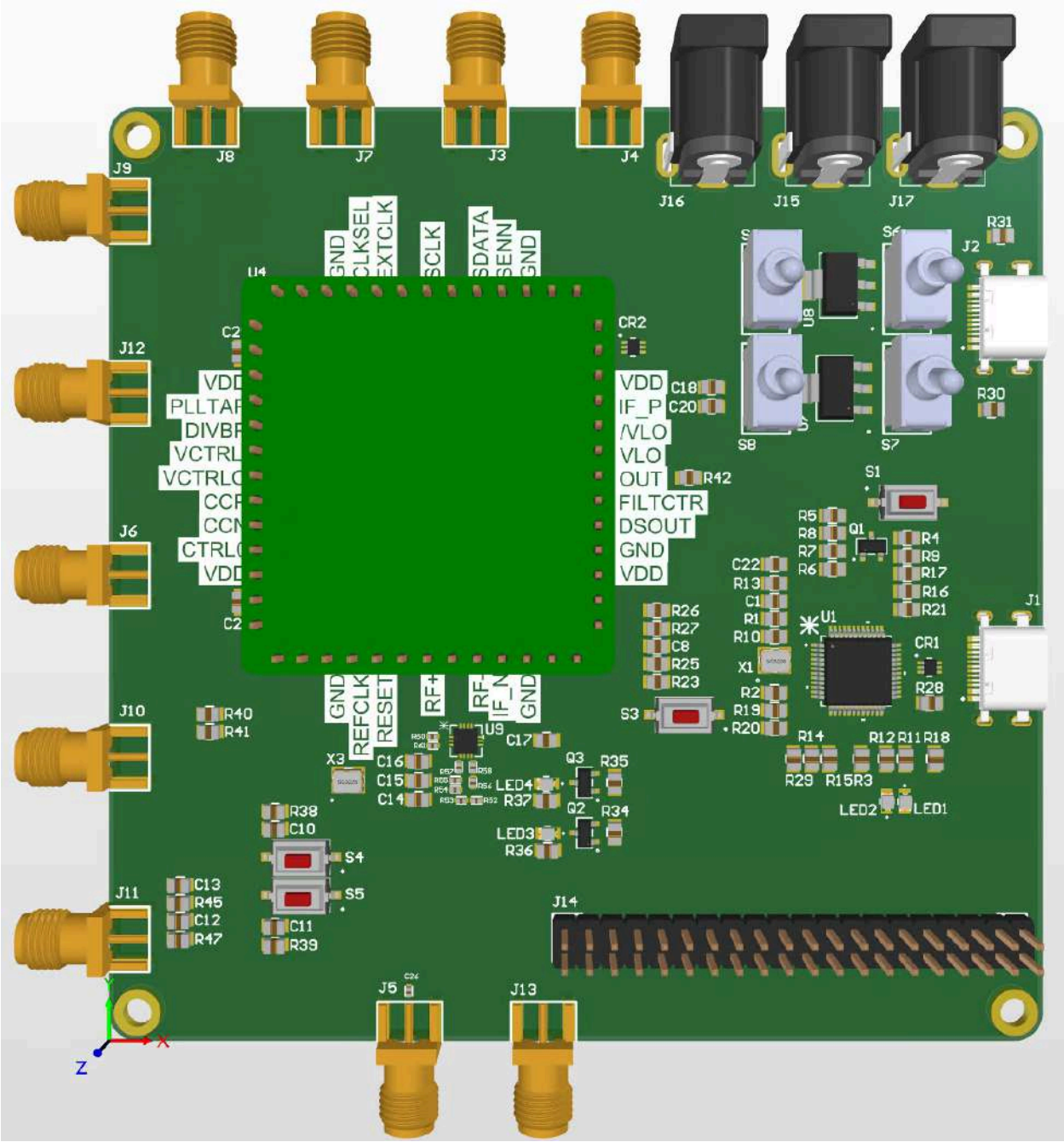


Figure 2: 3D View of PCB Board

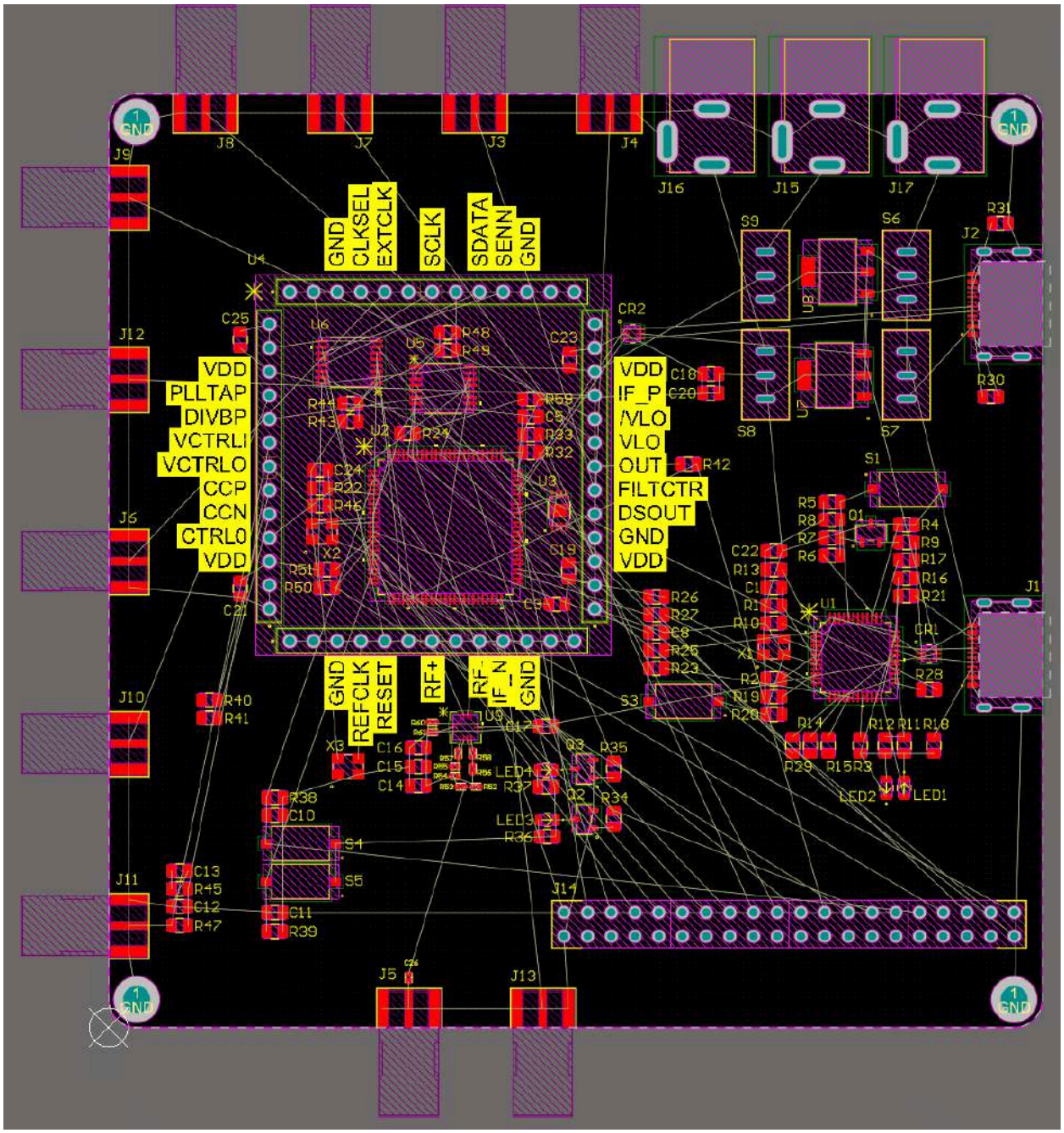


Figure 3: 2D View of PCB Board

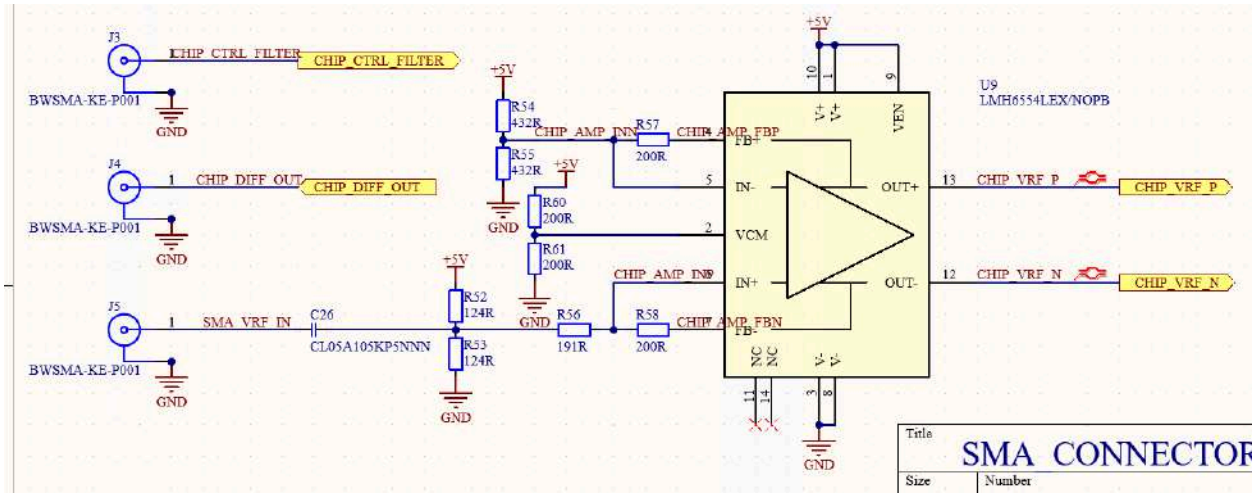


Figure 4: Analog Buffer Design of VRF Signal

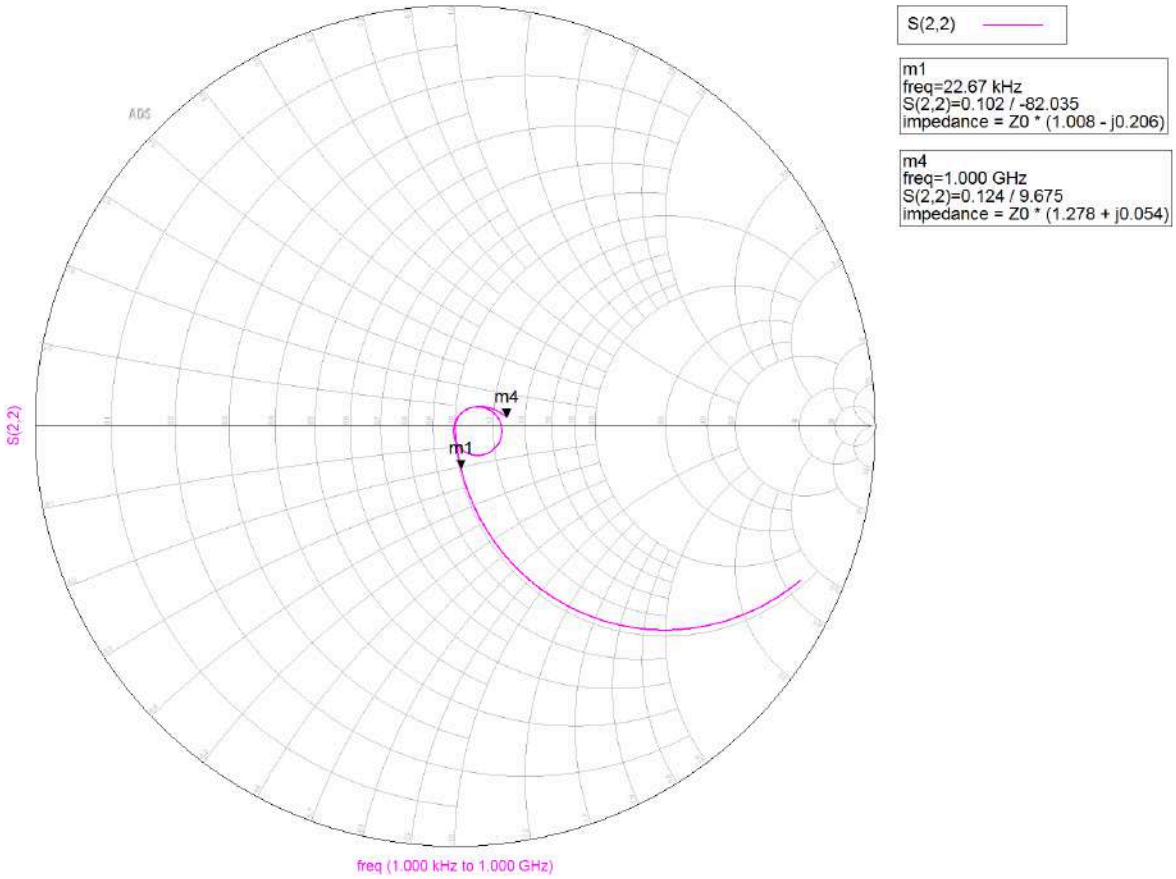


Figure 6: Layout Simulation of Impedance on VRF Input Sweep from 1 kHz to 1GHz.

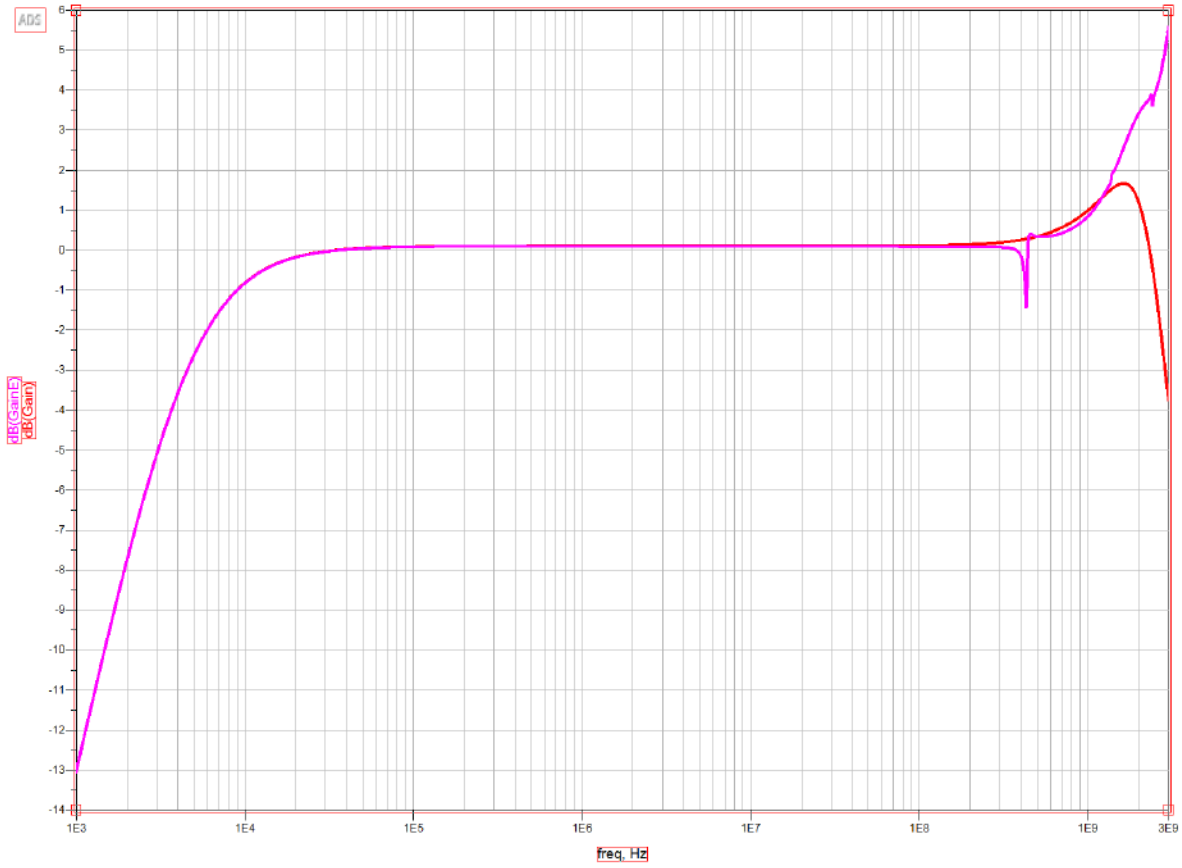


Figure 9: Layout and Schemtatic Simulation of Figure 4, Red is Schematic, Blue is Layout

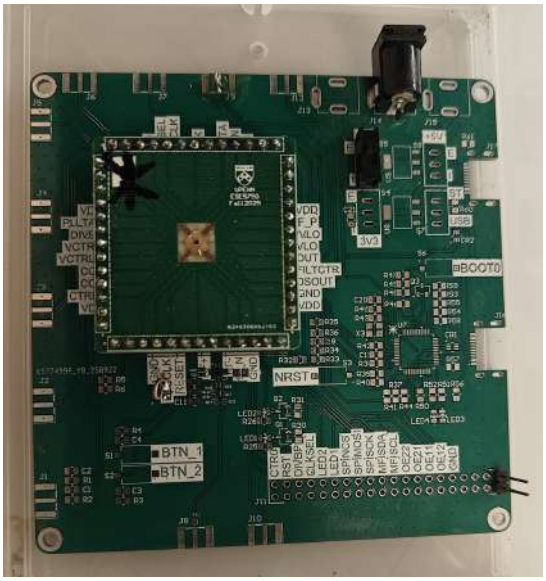
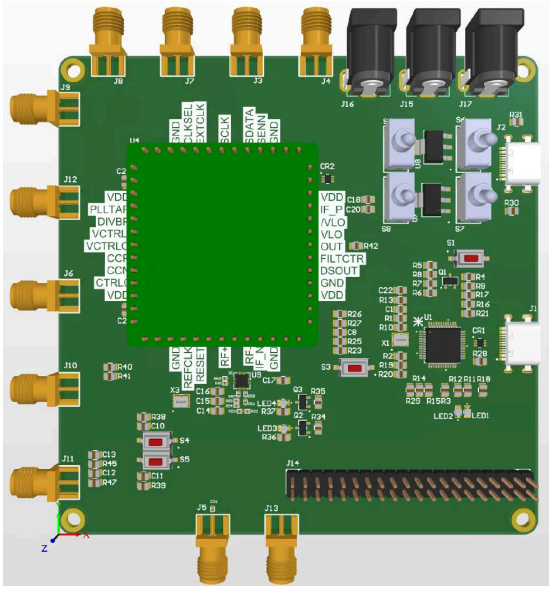
University of Pennsylvania
Department of Electrical and System Engineering

Chips Measurement

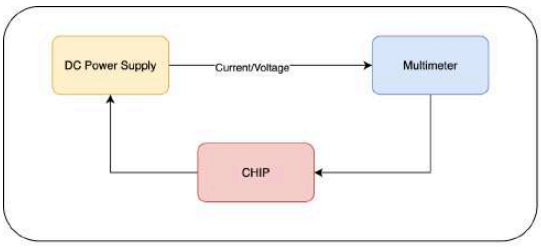
Abhik Kumar 57295964
Zonghua Ouyang 39907711
Team: 4
TA: Bryce Yu

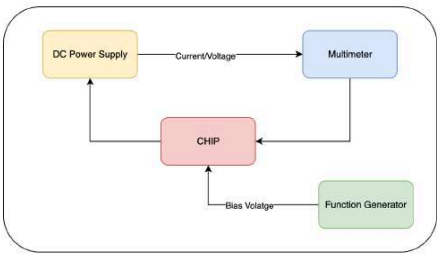
DC Measurement

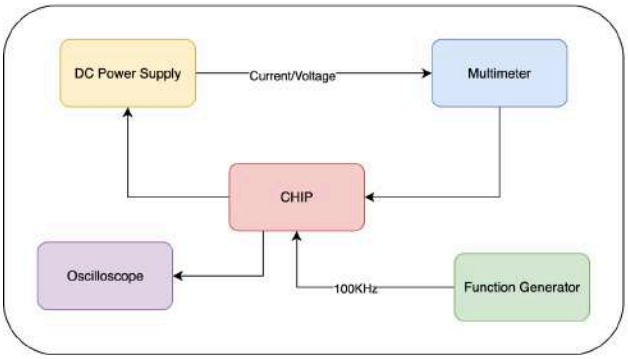
Hardware Setup

Carrier Board Picture	Carrier Board Schematic and Pinout
	

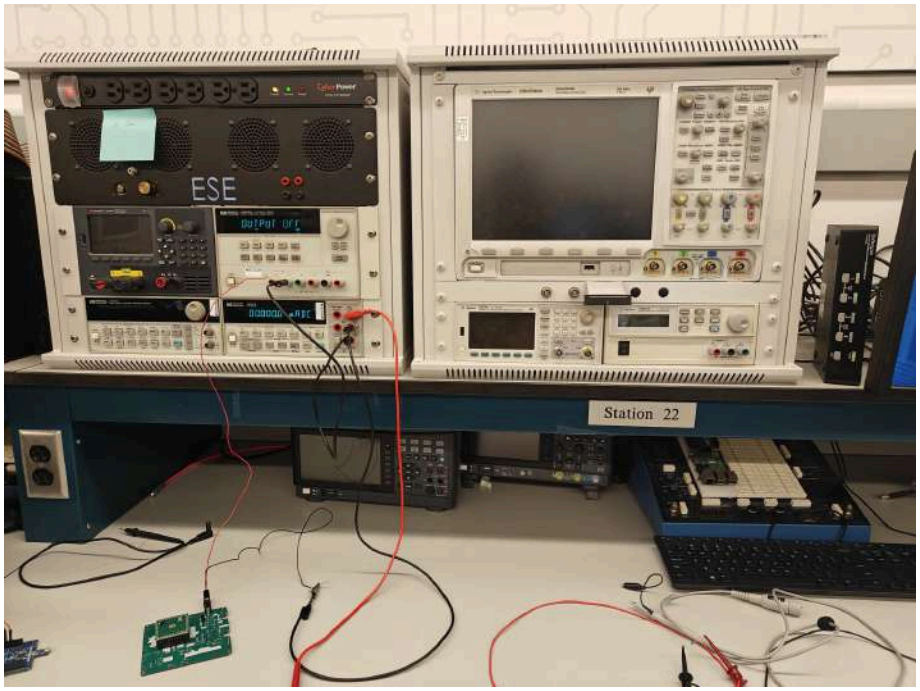
- **DC Measurement Setup Block Diagram / Schematic**



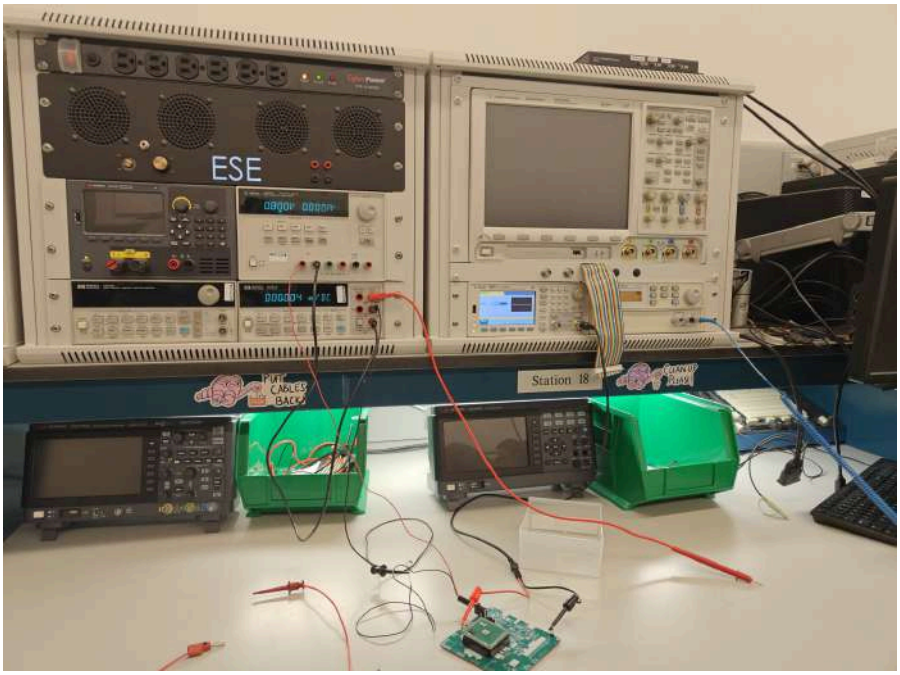




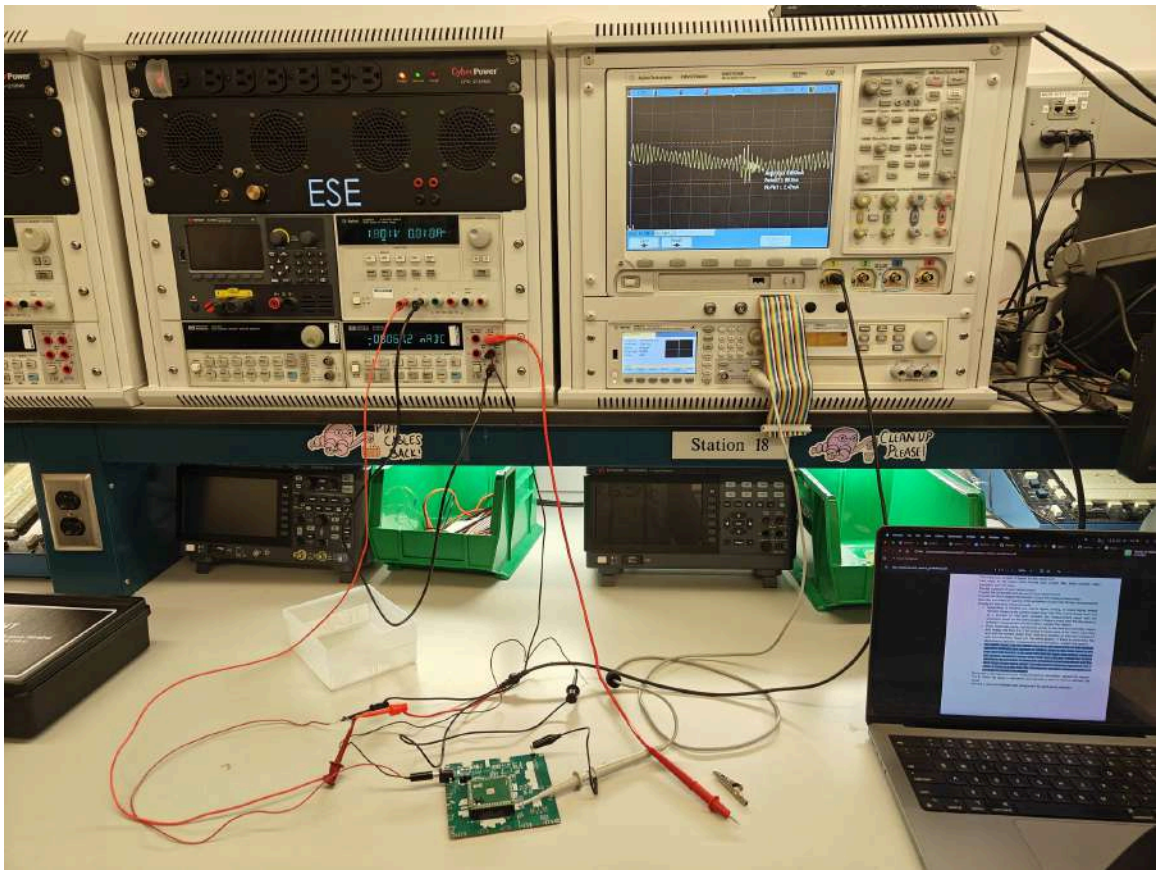
- **DC Measurement Circuit Setup**



Setup for Sweeping VDD



Variable Bias Setup



Setup for 100KHz clock frequency

ESD Protection Procedures

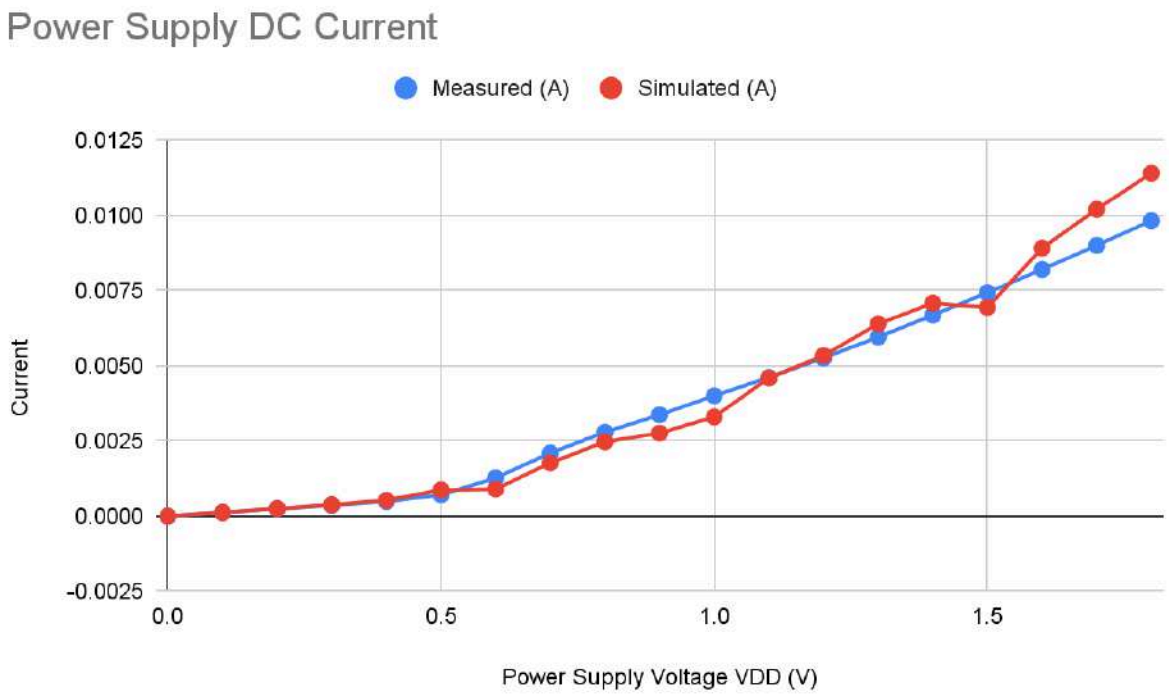
1. Grounded Workstation
    - Performed all measurements on an **ESD-safe mat** connected to earth ground.
2. Wrist Strap Use
    - Wore a **grounded anti-static wrist strap** at all times while handling the chip or connecting probes.
3. ESD-Safe Equipment
    - Used **ESD-safe tools**, including tweezers, cables, and probe tips.
    - Ensured test instruments (oscilloscope, power supply, multimeter) had **common ground connections**.
4. Proper Handling of Chip and Board
    - Handled the chip and carrier board **only by the edges**; avoided touching exposed pads or pins.
    - Stored the chip in **anti-static bags or conductive foam** when not connected.
5. Power Supply Precautions
    - **Set the power supply to 0 V before connecting** Vdd and GND lines.
    - Gradually ramped up voltage to avoid transient spikes.
6. Ground First, Then Power
    - Always **connect the ground line first**, before Vdd or signal lines, to ensure a stable reference and prevent floating grounds.
7. Environmental Control

    - Kept the measurement area **free from dust and humidity**, minimizing surface charge buildup.
8. Limited Physical Contact
    - Avoided frequent plugging/unplugging of cables or probes while the system was powered.
9. Discharge Before Handling
    - Touched a grounded metal surface before handling any component to **discharge body static**.
10. Post-Measurement Care
    - Powered down the system before disconnecting the chip.
    - Stored the chip and board back in an anti-static packaging/plastic box.

Measurement Results and Analysis

- **Vdd Sweep (General)**

  Plot: Current Drawn vs. Vdd (Measurement & Simulation)

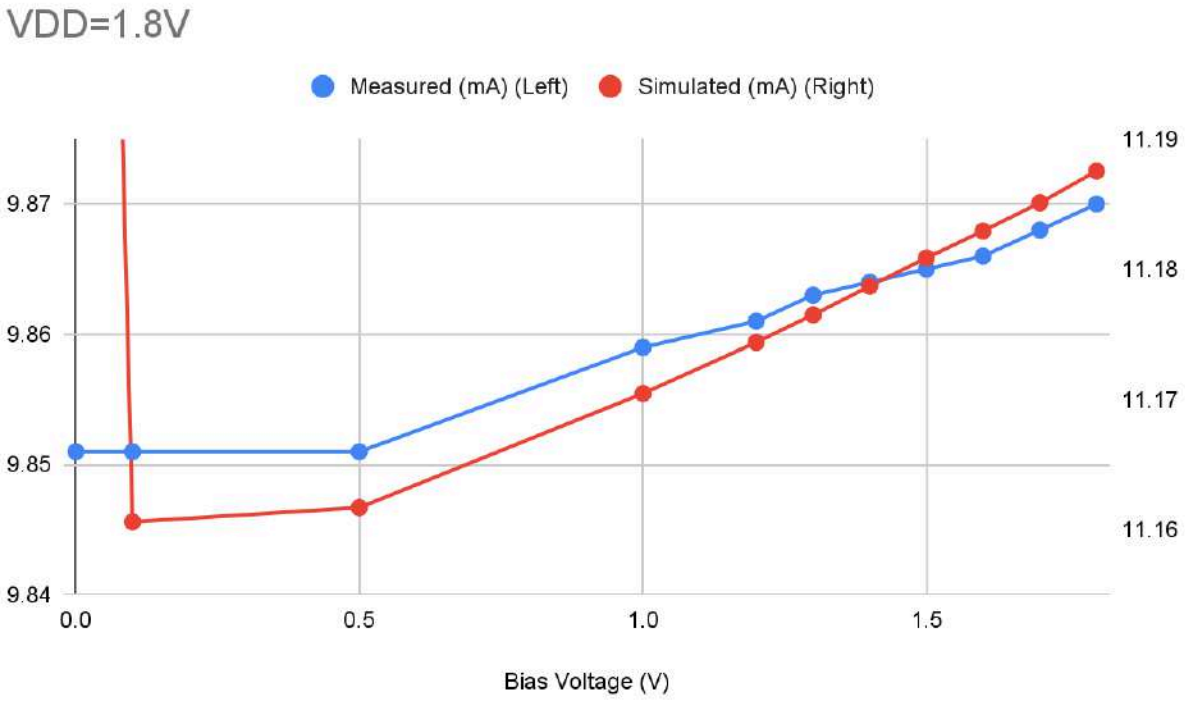


- Discussion of results and discrepancies

The discrepancy between the measured current and the simulated current is about 20%. The reason for this discrepancy, I guess, is that the value in the control register is random when powering on, which may affect the power consumption. We also observed that the current is influenced by the method that the chip was powered on. Using the power button on the DC power supply (increasing the Vdd gradually) will have a higher power consumption than using the switch on PCB (increasing the Vdd suddenly).

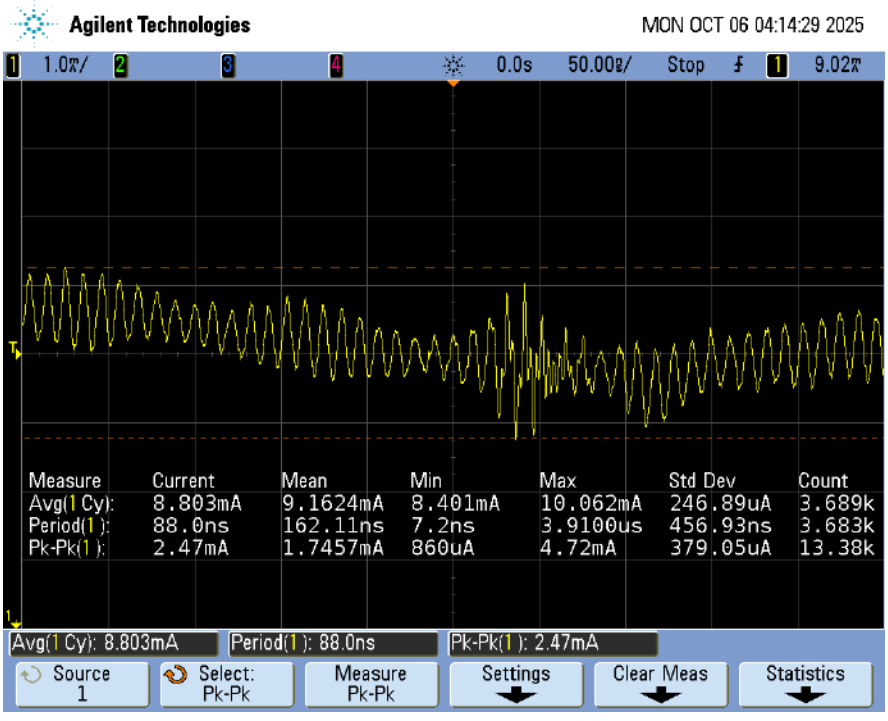
- **Bias Point Measurements (If Applicable)**

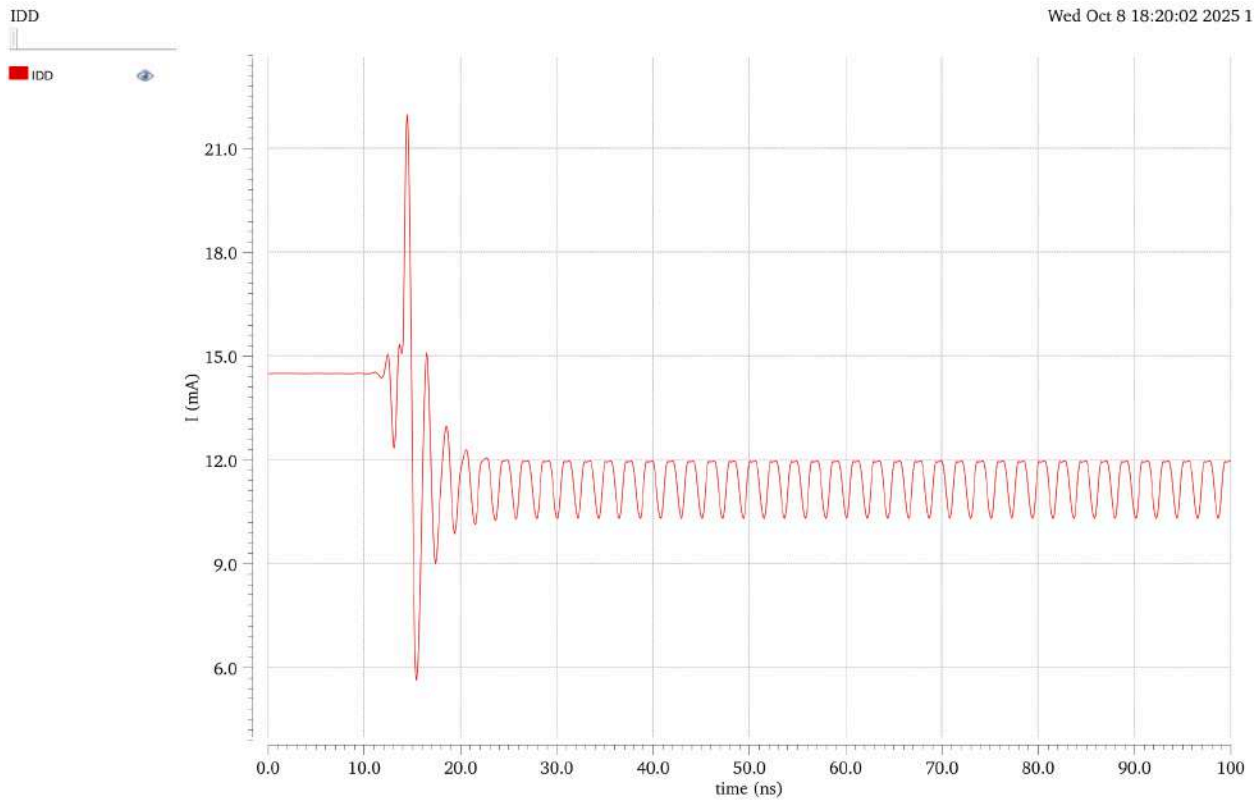
The graph below is measured by providing a power supply of 1.8 V and sweep the bias voltage. We didn't follow the guideline, which requires us to sweep the Vdd, because our chip could be damaged when the VDD is lower than the bias point. In that case, the ESD protection diode will be overloaded and broken.



We also tested the result at 0.8 and 1.2 VDD to test the results, which was very similar to expected result.

Digital Chip Current Waveforms (If Applicable)





With 100Khz the results remained the same for the measurements and we are able to only observe noises in the oscilloscope.

Internal VCO provides a frequency of about 600 MHz. A current change with that high frequency will be filtered out by the bypass capacitor within our chip.

Task Assignment

- We together did the DC testing and simulation of the chip

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Chips Measurement

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Team: 4
TA: Bryce Yu

1. **Write a couple of paragraphs on the importance of your chip and two paragraphs on your measurements and what your chip has accomplished.**

The chip designed in this project represents a critical step toward validating custom digital circuitry under real hardware conditions. Although simulations provide valuable predictions, fabricated silicon often exhibits physical effects—such as IR drop, parasitic capacitances, leakage, and process variations—that cannot be fully modeled in pre-silicon analysis. By characterizing the chip with laboratory measurements, we gain insight into how the design behaves when driven by actual voltages, clocks, and loads. This helps verify the robustness of the architecture, confirm power and timing assumptions, and identify discrepancies between simulation and real performance.

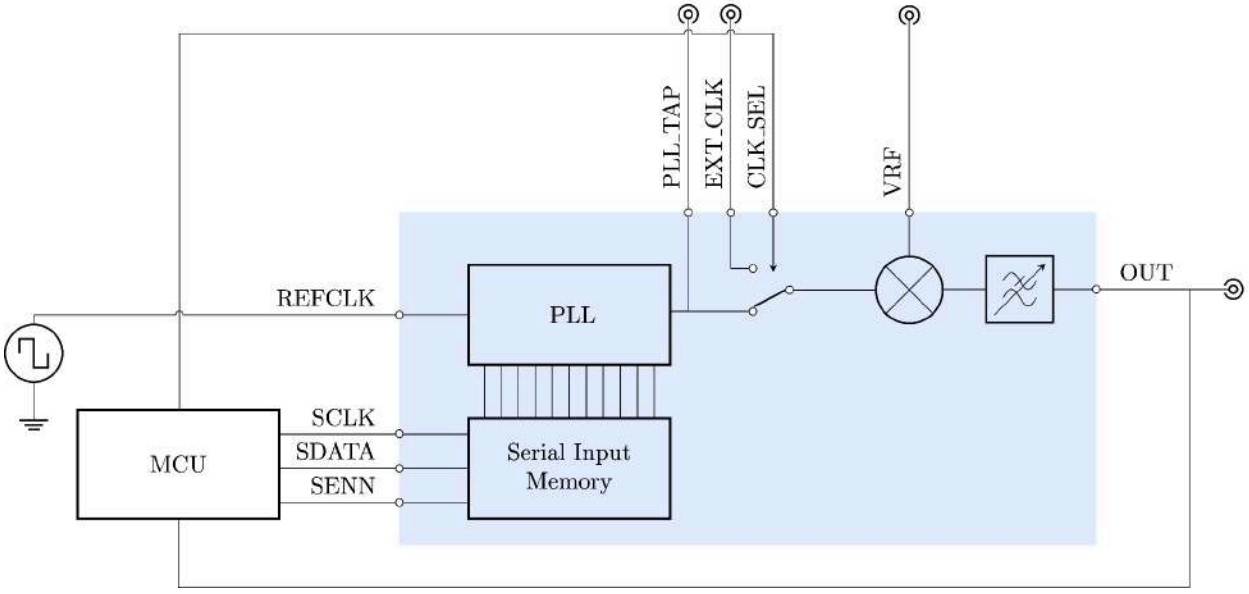
Beyond verifying the design, the chip also serves as an educational and practical platform for developing hands-on measurement and debugging skills. Working with real hardware requires understanding instrument limitations, proper ESD protocols, and precise data collection. The inclusion of spectrum analyzer measurements—examining the chip's output frequency content and clock harmonics—adds another layer of insight by allowing us to study signal integrity, noise coupling, and spectral behavior. These skills and insights are essential for modern semiconductor development, where designers must integrate both circuit theory and practical measurement expertise.

Our measurements focused on evaluating the chip's static and dynamic behavior through a combination of DC power characterization, transient waveform analysis, and spectrum analyzer testing. Vdd sweep measurements provided information on leakage currents, bias conditions, and overall power scaling. Time-domain current waveform measurements at 0.8 V, 1.2 V, and 1.8 V—with a — kHz input clock—confirmed that the chip's internal logic switches in synchronization with the clock, as seen by the repeating current pulses. Comparing measured current waveforms to simulated ones allowed us to identify small mismatches due to parasitics and non-idealities in the test setup.

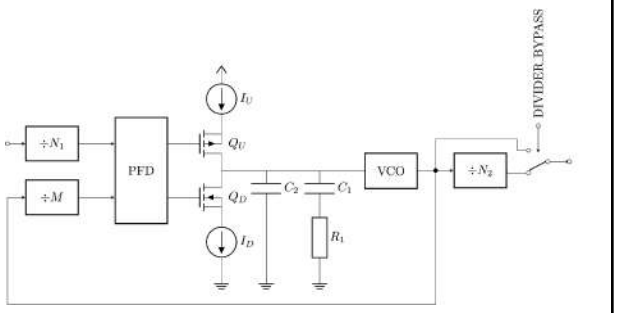
The spectrum analyzer measurements further demonstrated the chip's correct operation by revealing the expected clock fundamental frequency and corresponding harmonics generated by digital switching activity. Observing clean peaks at the expected frequencies confirmed that the clock distribution network and output stages were functioning properly. Additionally, the spectral data allowed us to evaluate noise, unwanted spurs, and potential EMI contributors in the design. Taken together, these measurements show that the chip performs its intended

functionality reliably, with power consumption and spectral characteristics closely matching simulation predictions, thereby validating the design and implementation.

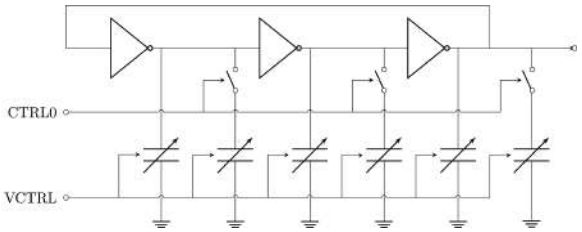
2. **Provide a detailed system block diagram.**



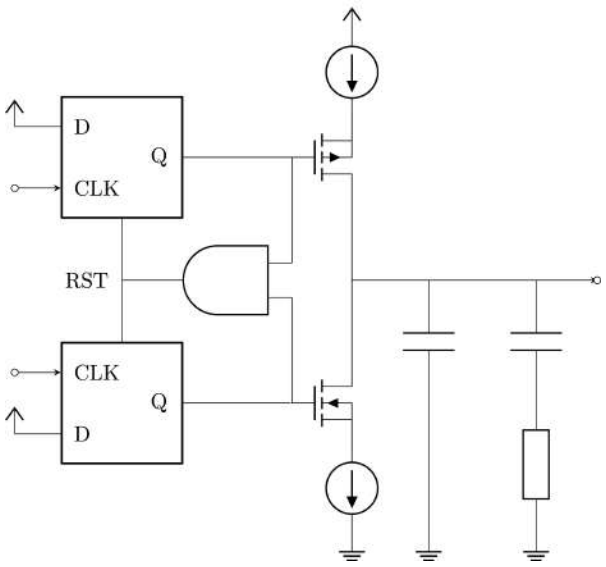
Overview

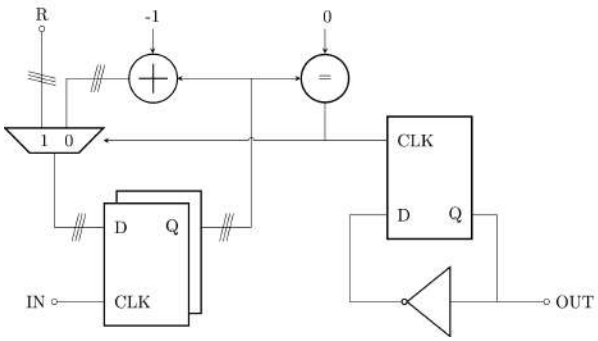


PLL

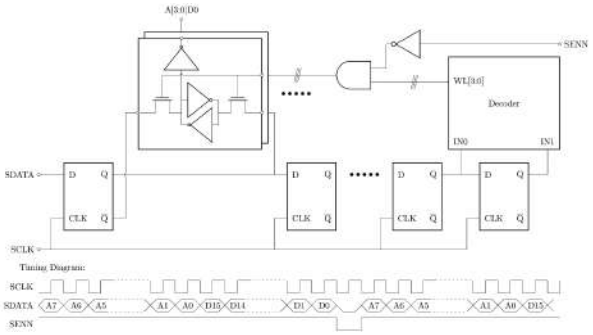
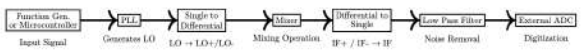


VCO

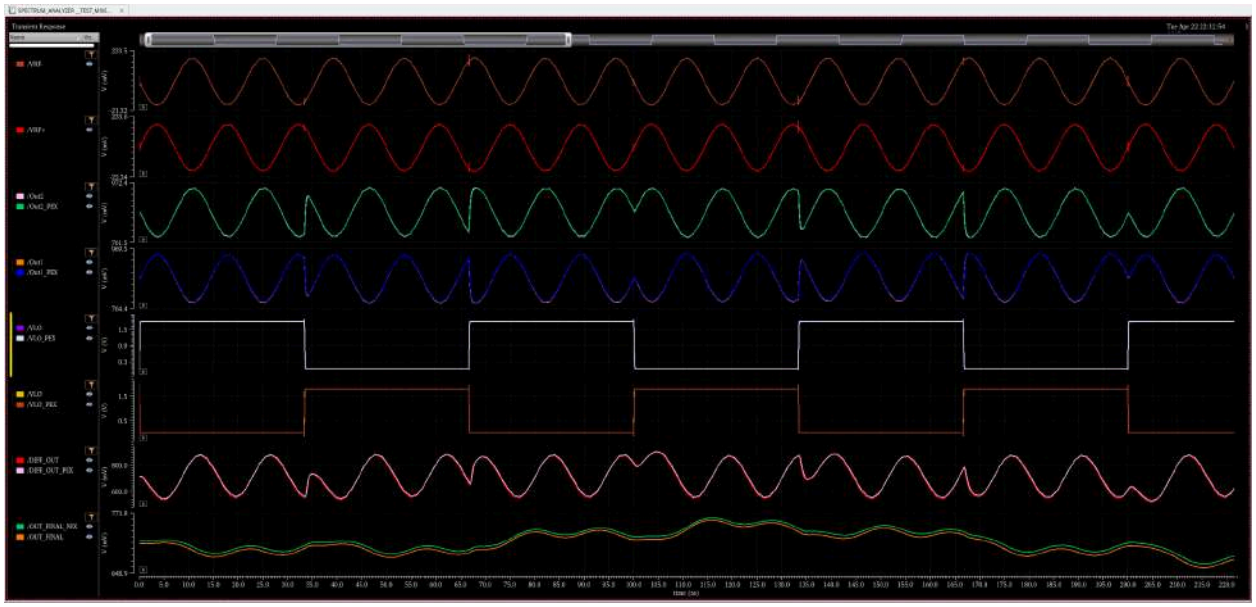




Divider

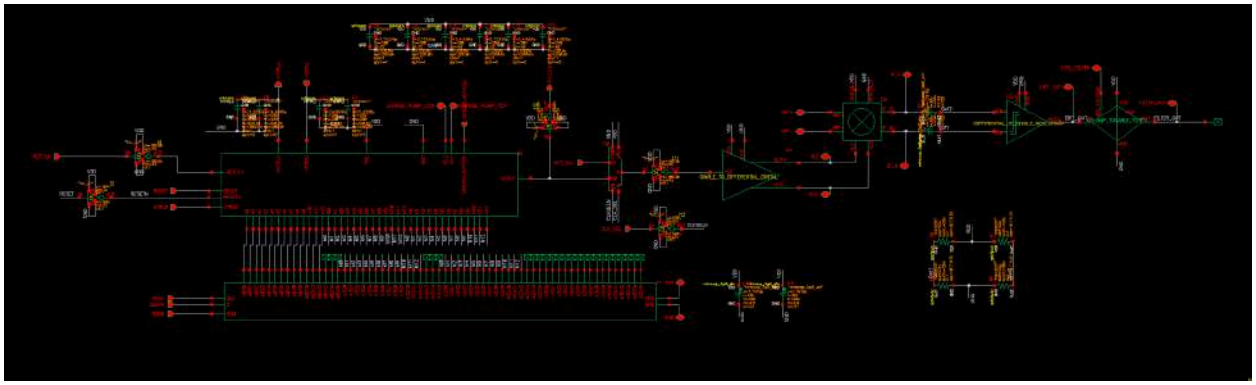
PFD	
 Serial Input Memory	 Block Diagram: Signal Path Through the Chip to External ADC

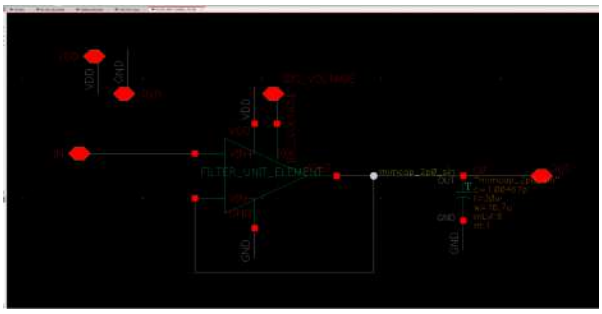
3. **Provide a top-level simulation of your block diagram and note the specifications of each block within the system.**



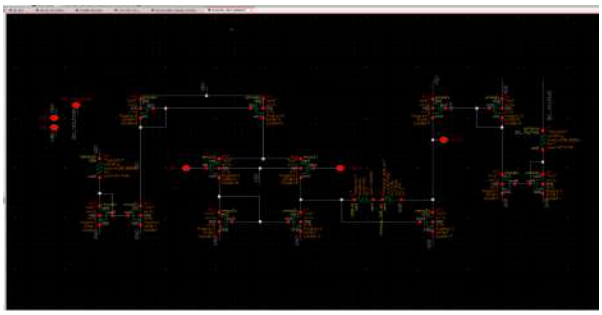
Result comparison

4. **Provide the detailed chip schematic and circuit schematic of each block.**

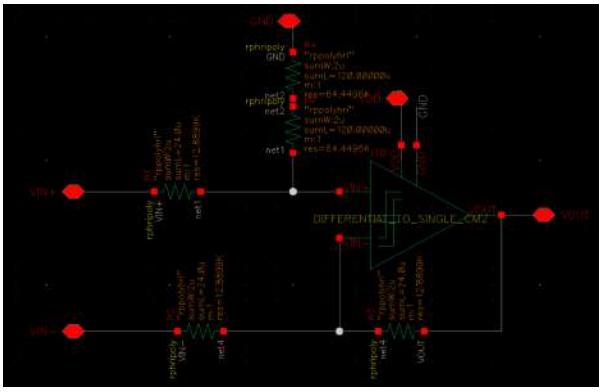




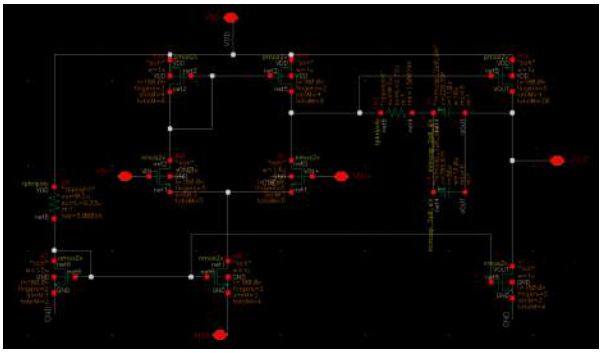
Tunable Filter



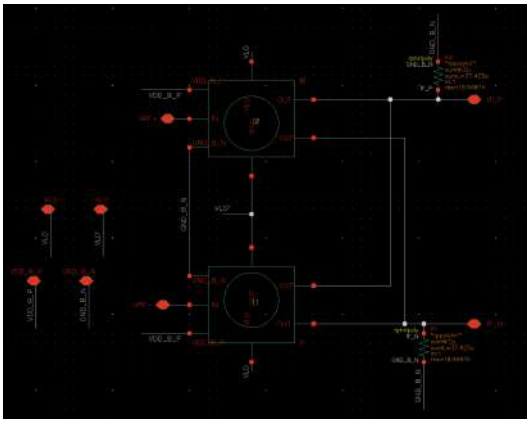
OP-Amp Circuit for Filter



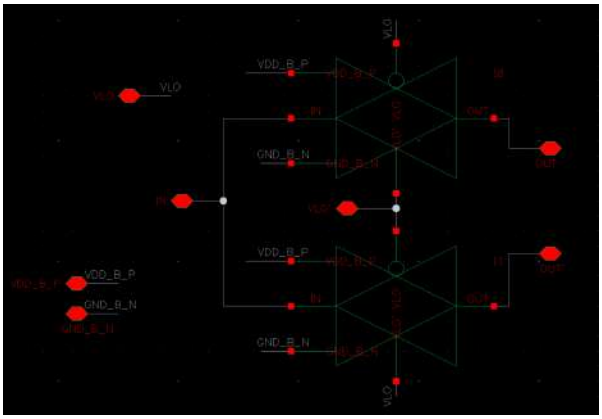
Differential to Single Convertor



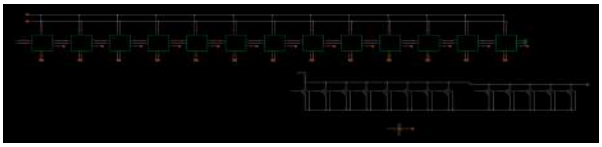
OP-Amp Circuit for D-S



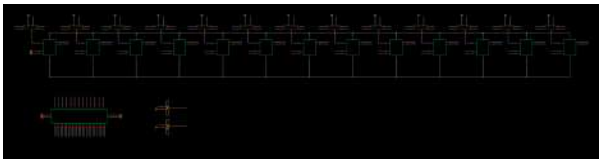
Mixer



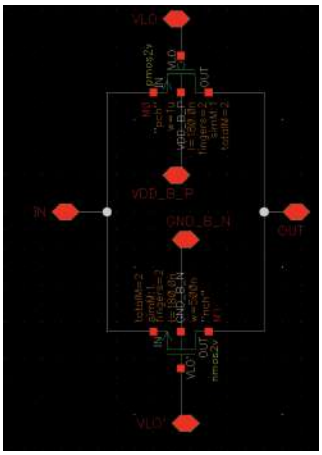
Mixer Blocks



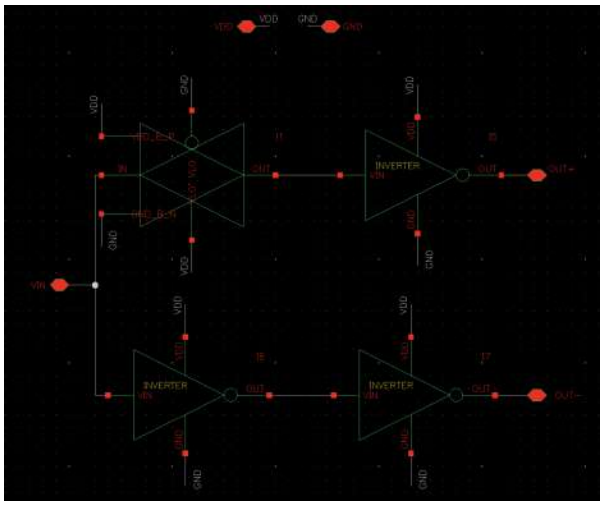
13-Bit M1 Memory



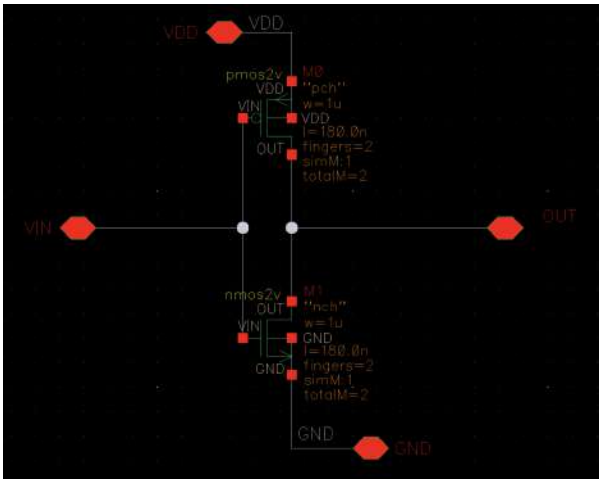
13 bit Register



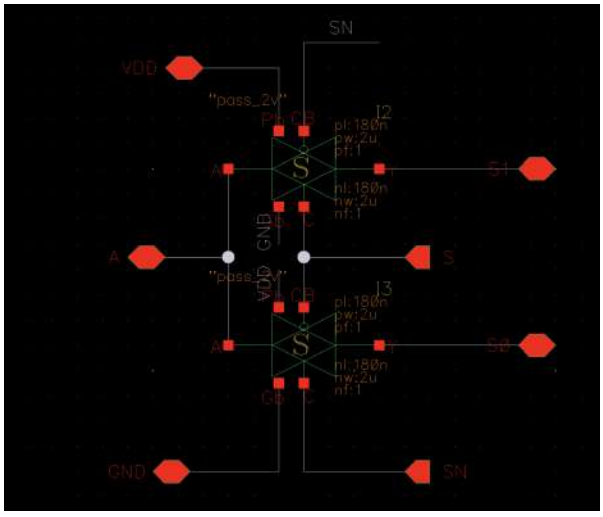
Switch for mixer



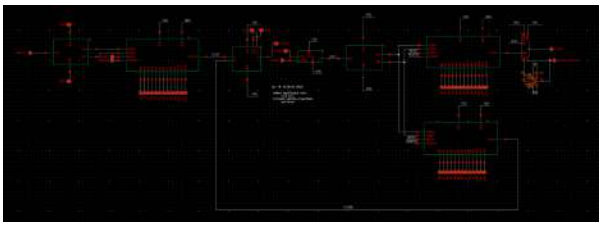
Single to Differential Digital



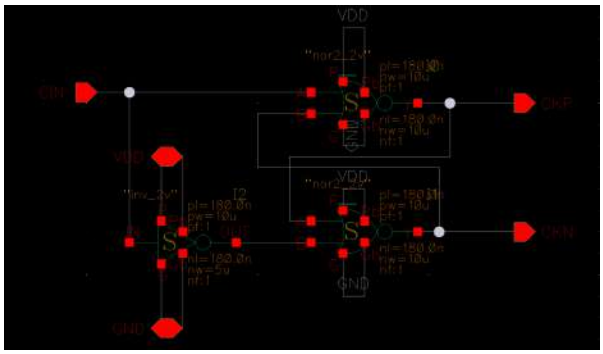
Inverter



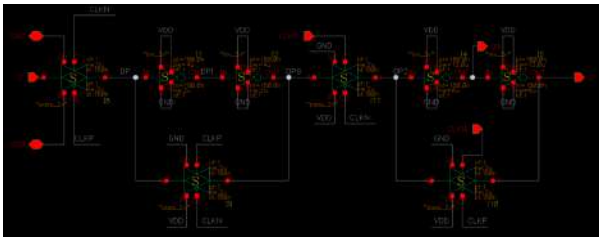
MUX



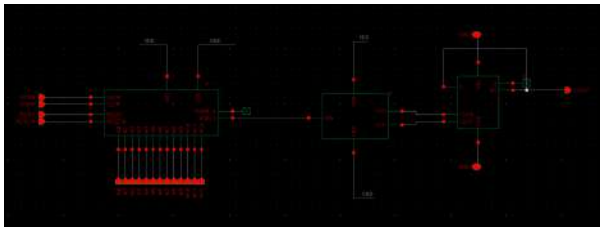
PLL



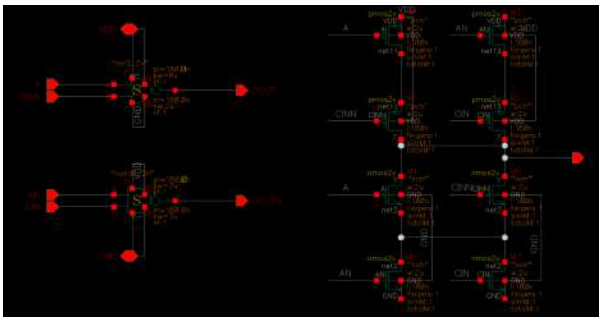
Non- Overlapping CLock



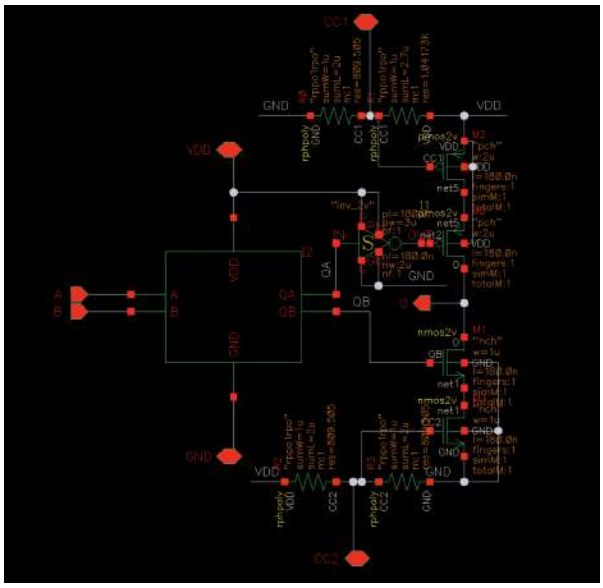
Flip- Flop



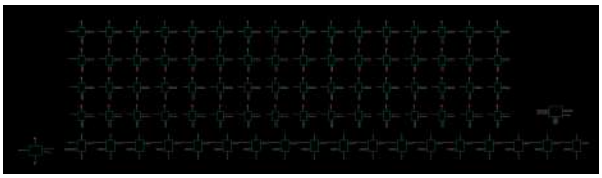
13bit Divider



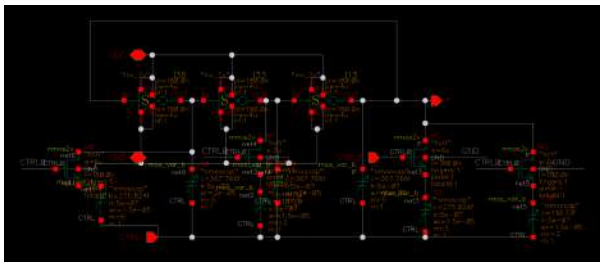
1Bit - Memory



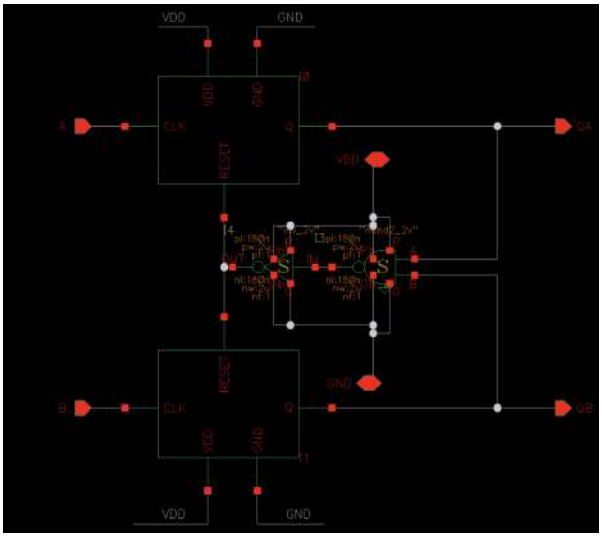
Charge Pump



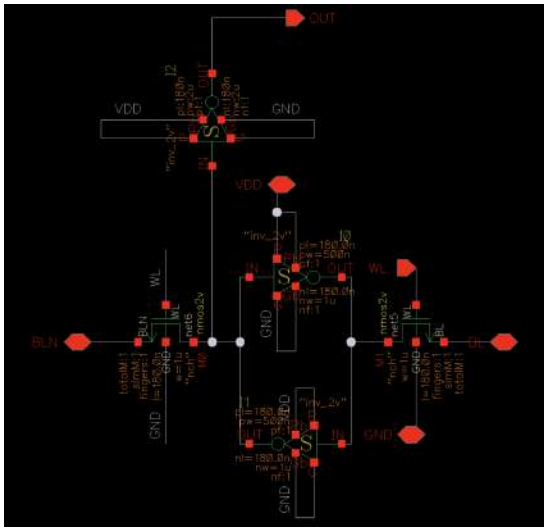
SPI Register



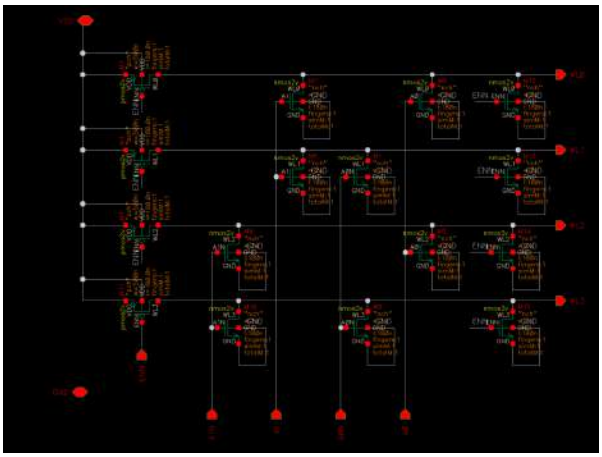
VCO



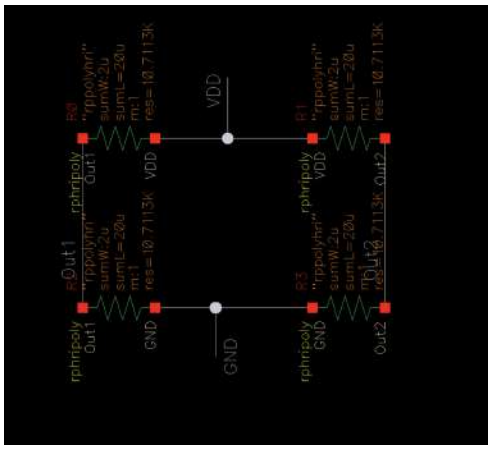
PFD



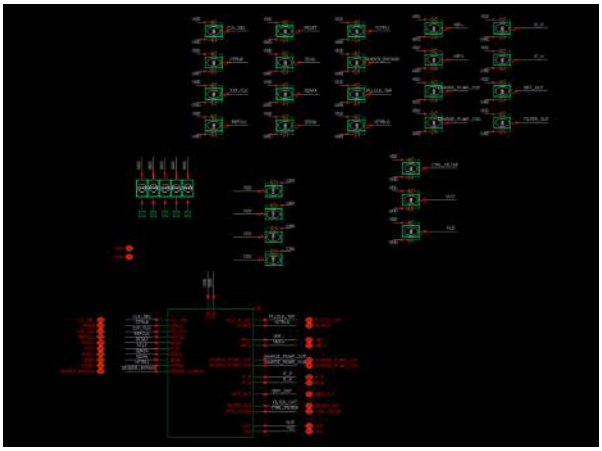
SRAM Cell



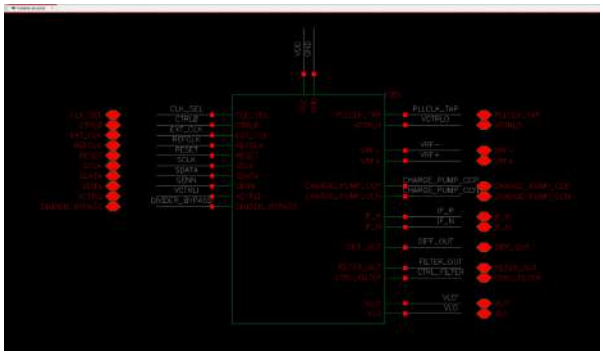
2Bit Decoder



Bias Circuit



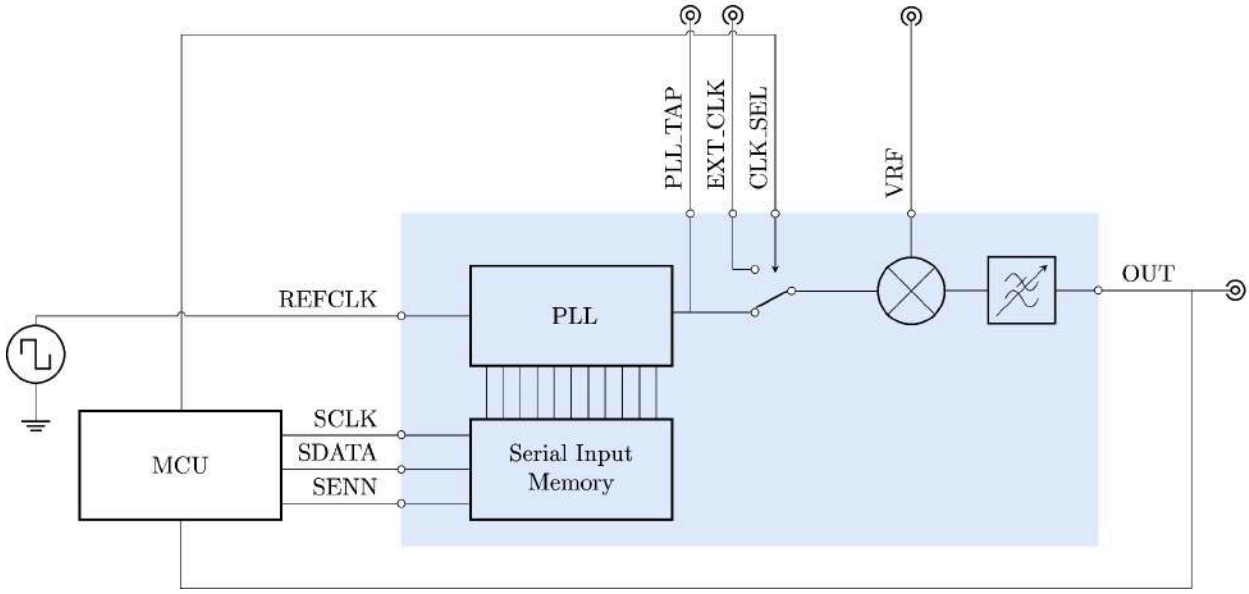
Chip With Pad



Top Cell Block

5. **Provide full post layout chip simulation results.**

6. **Provide details on each measurement setup. Include relevant block diagrams and equipment model numbers. Provide the schematic of your PCB and the details of the connections between your PCB and different equipment for each measurement.**

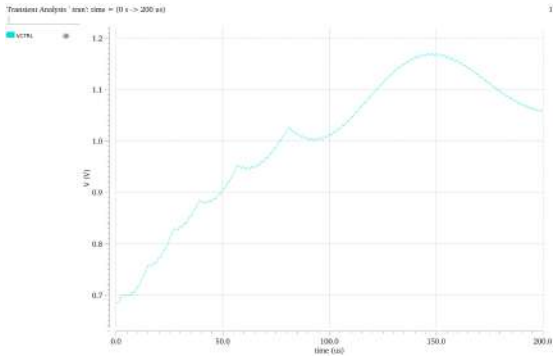


Measurement Setup

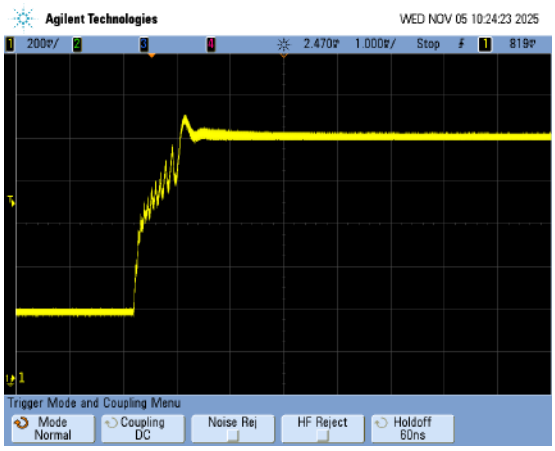
PLL_TAP, OUT is connected to an external oscilloscope, VRF is connected to a signal generator.

7. **Explain each conducted measurement in detail and compare each measured result with the corresponding simulation result. If there are discrepancies between the simulation results and measurements, clearly explain the reason.**

   PLL:

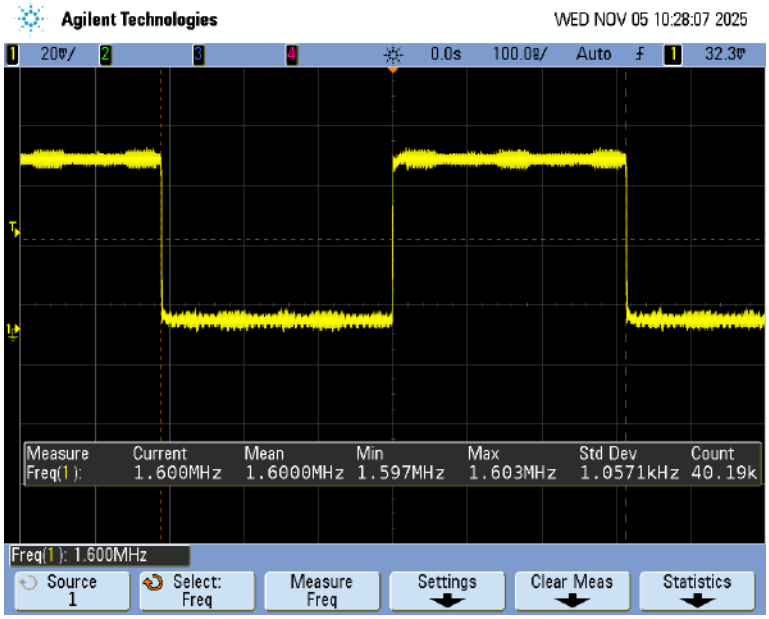


Simulated VCTRL



Measured VCTRL

The measured VCTRL matches the simulated VCTRL



Measured PLL_TAP

Simulated PLL_TAP

The measured PLL_TAP matches the simulated simulation, a pure square wave.

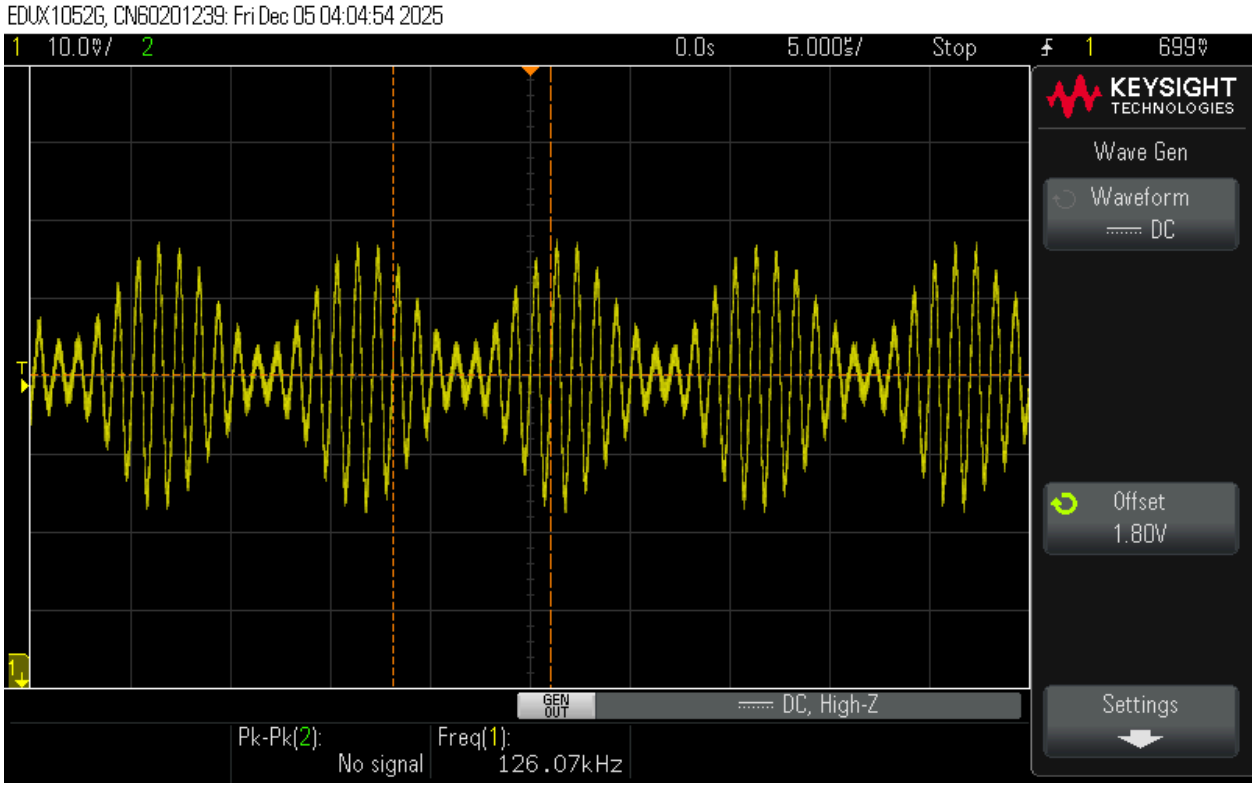
Measured Spectrum of PLL_TAP with bandwidth of 100 kHz

Offset (kHz)	0	1	10	100	1000
Phase Noise (dBc)	0	-30.5	-31.5	-56.34	-82.87

Measured Phase Noise

8. **Provide a detailed table of comparison between the proposed metrics and the measured metrics and comment on discrepancies.**

Parameters	Proposed	Measured	Discrepencies
Frequency Range	1~100 MHz	0.1~100 MHz	
Frequency Resolution	100 kHz	100 kHz	
Dynamic Range	80 dB	30 dB	High noise from the low pass filter.



When we pass the input frequency with a modulated wave our spectrum analyzer can separate out the modulated wave from the carrier wave.

9. **Provide a clear and detailed description of tasks conducted by each group member from beginning to end of simulations and measurements.**

Zonghua Ouyang:
Worked on the pll and simulation and measurement, Designed the app for control of the MCU for the measurement
Abhik Kumar:
Worked on Mixer+ filter simulation and measurement

We combined worked on the PCB and testing

<table>
<tr><th>PIN Name</th><th>Signal</th><th>Operation</th></tr>
<tr><td>CTRLF (DC bias)</td><td>0 - 1.8V</td><td>Filter Bandwidth Control (higher is better)</td></tr>
<tr><td>Vref</td><td><table>
<tr><td>Freq</td><td>> PLL signal</td></tr>
<tr><td>Amplitude</td><td>0-1.8V</td></tr>
<tr><td>offset</td><td>900mV</td></tr>
<tr><td>Imp</td><td>High-z</td></tr>
</table></td><td>Reference signal for mixer (onboard single to diff)

At higher frequency the amplitude goes low that is very hard to detect by the ADC and</td></tr>
</table>