Abhik Kumar

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Education

University of Pennsylvania **August 2024 - Present**
Master's of Science in Electrical Engineering – 3.91 / 4 CGPA *Philadelphia, U.S.*
Courses: *Embedded Systems, Digital Integrated Circuits & VLSI, SOC Architecture, Chips Design & Measurement, Mixed Signal*

Delhi Technological University **August 2019 - May 2023**
Bachelor of Technology in Electrical Engineering [CompE minor] – 8.73 / 10 CGPA *Delhi, India*
Courses: *Deep Learning, AI, Microprocessors & Microcontrollers, Digital Circuits System, Power Electronics, Operating Systems*

Skills

Programming Languages: Embedded C, C++, Golang, Ruby, Matlab, Python, NodeJs, HLS, SV, TCL, RISC-V
Protocols & Technologies: XBee, SPI, I2C, RS485, UART, BLE, CAN, Nb-IOT, LoRa, MQTT, ROS, CMake, JTAG
Hardware:WINC1500, ATMega, Digital Multimeter, Oscilloscope, Logic Analyzer, Ultra96, Lattice FPGA, ELoad
Software/Tools: Altium, Microchip Studio, MPLabX, Linux, GDB, Visual Studio Code, GitHub, JIRA, Docker, STM

Professional Experience

University of Pennsylvania **January 2026 - Present**
Head Teaching Assistant, IoT Edge Computing *Philadelphia, PA, USA*

- Led TAs to architect an embedded IoT curriculum, building **FreeRTOS** and **Altium** (4-layer PCBA) lab modules.
- Mentored student hardware builds, debugging custom **ARM based** MCUs, **I2C/SPI** sensors, and real-time firmware.
- Developed bare-metal **C** optimized for seamless **RTOS** migration, guiding **35 teams** through **JLCPCB** manufacturing and **SiLabs/Azure/MQTT** integration, navigating the custom PCBs **load testing** running individualized firmware.

Head Teaching Assistant, IoT Wireless, Security, & Scaling **August - December 2025**

- Guided teams building IoT system on **STM32/Nordic**, debugging **Zephyr** across **LoRa**, **Cellular**, **Matter**, **BLE**.
- Developed **CI/CD** for **OTA** and **Secure Boot**, enforcing device-to-cloud security via hardware-accelerated **AES/TLS**.

MUNCH Industries, Inc. **June - August 2025**
Lead Embedded & Electrical Systems Engineer Intern *Philadelphia, PA, USA*

- Led the design and development of the electrical and embedded control systems, managing firmware architecture, power distribution, and **CAN-based** communication between multiple microcontrollers and Backend support.
- Developed **Zephyr** firmware using **devicetrees**/interrupts for cloud APIs, validated via **HIL** and `ztest` mocked drivers
- Automated **CI/CD** via Docker/Git, reducing bugs by **30%** and accelerating hardware integration iterations by **40%**.

Cogoport **January - September 2023**
Software Development Engineer (Full Stack Developer) *Gurgaon / Mumbai, India*

- Engineered a streamlined onboarding platform with automated data population across 5 Asia-Pacific nations (ID, VN, TH, SG, CN), cutting manual effort by **70%**, reducing errors by **30%**, and tripling user engagement.
- Deployed **Leaflet** cargo maps and CRM for **2,000+** users, accelerating updates by **20%** & reporting accuracy by **40%**.
- Automated agent allocation via predictive shipment forecasting, boosting retention by **60%** and revenue by **30%**.

Research & Project work

Pipelined RISC-V Processor Design **January 2026 - Present**

- Architected a custom pipelined **RV32IM RISC-V** core with integrated **data cache** in **SystemVerilog**.
- Engineered **branch prediction**, **out-of-order** execution, and **bypass/stall logic** to resolve pipeline **data hazards**.
- Synthesized **RTL** via **Yosys** onto **FPGA**, debugged waveforms and validated logic using **Verilator** testbenches.

TSMC 45nm RISC-V SoC Tape-Out **January 2026 - Present**

- Generated custom **RISC-V SoC RTL** utilizing **Chipyard** generators to drive the automated physical design pipeline.
- Engineered an **RTL-to-GDSII** workflow via **mflowgen**, migrating flow from Foundation to Cadence **Stylus flow**.
- Executing fullchip synthesis & PnR on **TSMC 45nm** via **Calibre/Innovus**, validating **IR drop** and **Clock domains**

Real-Time Data Compression on Zynq SoC with ARM–FPGA Co-Design **August - December 2025**

- Developed a real-time **ARM–FPGA compression pipeline** on **Ultra96** (handling **SHA-256**, deduplication, chunking on **ARM/NEON**) and utilized **Vitis HLS**, **OpenCL**, and **XRT** to offload **LZW** to the **FPGA** via **AXI DMA**.
- Achieved **4× speedup** (**200 Mb/s**) via pipelined **LZW kernel**, validated using **HLS testbenches** and **Ethernet**.

RTOS-Implementation on custom 4-Layer PCB **January - May 2025**

- Designed a **4-layer PCB** in **Altium** (**SAMD21** MCU, **WINC1500** Wi-Fi, fabricated via PCBWAY) and developed **FreeRTOS** firmware drivers, a custom **CLI**, and **bootloader** for an automated irrigation system.
- Sensor Fusion with motor and pump over I2C; on **FreeRTOS** and WiFi alerts, boosting water efficiency by **40%**.
- Built a **Node-RED** dashboard for remote control and alerts, optimizing irrigation and cutting water use by **25%**.

Reinforcement Learning in Simultaneous Localization and Mapping **Springer Nature, April 2025**
Authored a Springer book chapter on model-free RL and SLAM-based path planning for reconfigurable robotic systems(ROS).